THE ELECTRONICS MAGAZINE WITH THE PRACTICAL APPROACH

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Elektor Electronics

Video Mixer

Mini EPROM Programmer

Simple AC Millivoltmeter

HC Oscillators

8052 modification

CMOS Preamplifier (2)

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January 1990
Volume 16
Number 174

Theme of the month in February will be Audio & hi-fi

Also in the February issue:

- Dark room clock
- Video mixer (Part 2)
- Car theft deterrent
- Current sensors
- Feedback killer
- Capacitance meter
- PC radio
- Waveform modulation of the mains voltage
- Initialization aid for printers

Front cover
A software engineer inserts a microprocessor board into a Voyager CD-ROM jukebox disc library that has been designed and built by Next Technology Corporation of Cambridge.
Voyager is a floor-standing unit intended to slide under or stand alongside a desk and has a capacity for up to 270 compact discs and 8 CD-ROM drives.
Each CD can be used to hold large amounts of information, such as text, video or sound that can be retrieved quickly by a computer. In computer terms, it can hold over 175 Gigabytes of information.
The British Library uses the system as part of the Adonis project, which stores over 200 biomedical journals on CD-ROM.

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RADIO MAKES A COMEBACK

Wouldn't it be convenient not to have to change frequency when listening to news or your favourite music on the radio during a long car journey? Or to enjoy the same sound quality as you obtain from a compact disc, whether you are at home, in your car car or on the beach?

Thanks to modern technological developments, radio, sometimes considered as the poor relative in the broadcasting family, living since the second world war in the shadow of television, is making a comeback.

Since the introduction of FM in Stockholm in 1952 and of stereo broadcasts sometime later, radio had not undergone any spectacular development until very recently. But now it is radio's turn to take advantage of the progress made by modern technology, digitization, artifical intelligence, microchips, and so on.

RDS and DAB: two keys to the future of radio

What is RDS?

RDS, or Radio Data System, is a new, radical invention whereby digitized information is added to FM transmissions. In simple terms, it is a code given by the broadcaster enabling any radio receiver to recognize a particular type of programme, the frequencies on which a given station is transmitting, traffic information or even personal messages.

Say that you want to listen to a play. Your receiver will automatically scan for, and stop at, the station that is broadcasting a play at the time. In practice, this means that classical-music fans will not have to look for their favourite music programmes on other stations when the one they are listening to finishes. Once preprogrammed by the user, the receiver will do it for him, thus providing hours and hours of uninterrupted classical music.

Thirty types of programme had already been identified by the European Broadcasting Union (EBU) in January 1988, 15 of them pre-defined (news, current affairs, information, sport, education, plays, culture, science, variety programmes, pop music, rock music, light music, light classical music, other music) and 15 others left free for the broadcaster to decide. A further programme, called the '31 alarm' is set aside for the future broadcasting of distress messages concerning, for example, pollution, a chemical leak or other hazards. This is what is called the PTY (programme type), which indicates on the display the type of programme currently being broadcast.

However, the capabilities of the RDS do not stop there. You are on the motorway and a news flash concerning local traffic interrupts your programme, your cassette or your compact disc, or even switches the receiver on if it is switched off, to inform you about a bad traffic jam, an accident, roadworks, or any other events that could affect your route. Not only will this make the journey easier, it may well help to relieve congestion on the roads. As soon as the announcement is finished, your programme comes back on again or your radio switches itself off. This capability is called TA (Traffic Announcement Identification). As soon as the signal indicating a traffic announcement is received, it is given priority and the radio switches over accordingly.

The transmission of traffic messages is not completely new. A forerunner to the system, called ARI (Autofahrer Rundfunk Information – Vehicle Drivers' Radio Information), has been broadcasting this type of information for some years now in the Federal Republic of Germany and Austria. Compatibility of RDS and ARI in these countries has been ensured.

In Britain, the BBC is conducting a pilot experiment on five of its local networks, chiefly in the south-eastern part of the country. In the past, traffic information obtained by telephone or other means was forwarded to local radio stations and read out directly by an announcer. Since the ARI system did not exist in Britain, there was no link between the different sources of traffic information capable of providing a veritable RDS service.

One thus had to be created, involving police stations and the services supervising the roads and railways and air and sea navigation. Under the pilot project, each of the sources of information will have a computer equipped with the BBC's own software. It will thus be just as quick and simple to compile messages as it was by telephone. The messages will be received on computer in the newsroom that will be located in the BBC's traffic centre currently under construction at Broadcasting House in London. Once processed, they will either be made available to the local radios on a screen to be read by an announcer on the air or be broadcast by the BBC traffic centre over the RDS. Considerable technical and editorial lessons are expected to be learned from this experiment, which the BBC will be conducting until April this year.

Meanwhile, the RDS already offers a whole range of advantages. For instance, we now have the PS (Programme Service name), the identification number that, on reception, is converted into alphanumeric characters and displayed on the receiver. The listener can thus always identify the programme being received. A telephone number can be displayed for a "phone-in" programme, or an address for sending letters to the station. For road safety reasons, such messages are not intended for your car radio: an accident can so easily be caused by a few seconds of inattention!

The RDS also allows you to select specific programmes from a programme schedule. For example, if you do not want to miss the one o'clock news but fear that, with your mind taken up with preparing lunch, you will forget to switch your radio on at the appointed time. The PIN (Programme Item Number) will automatically switch on your radio receiver or video recorder preprogrammed to tune into or record the selected broadcast.

The RDS automatically adjusts your receiver's clock to summer time and takes account of time differences. The CT (Clock Time and date) uses universal time and modified Julian date with automatic correction for location, time zone and local time. CT will display the date and time.

You have no doubt noticed that the tone of a spoken broadcast is not always suitable for a music programme. The MS (Music Speech switch) indicates the type of programme (speech or music) and automatically switches to one of the two preset volume levels.

People who use a computer professionally or in the home will know that it uses digitized programmes and information. The RDS is also a vehicle for digitized information and can thus be used to transmit information from your radio to your computer. The TDC (Transparent Data Channel) is a channel set aside to display radiotext on a television screen or printer. Software and other data could thus be transmitted.

In all, the RDS may offer some 15 services that are already available, either wholly or partly, to listeners who have receivers equipped with appropriate reception circuits. Under certain conditions, digital data and analogue signals can be transmitted simultaneously on a single FM channel without interference. They are decoded on reception.

However, the prime advantage of the RDS, which is the main reason for its existence and prompted all the necessary research, is the PI (Programme Identification). The PI automatically finds the frequency of the station of your choice, thereby avoiding the annoying signal losses so frequently encountered during journeys over long distances. Radios equipped with an RDS system will not only select your station, but also the best frequency on which to listen to it. In other words, as you drive a fair distance, you change frequencies several times without even noticing and without touching your radio even once. Owing to propagation phenomena and the small coverage area of FM transmitters, travellers whose radios are not equipped with an RDS often have to search manually for a station on which their programme is most clearly audible. The PI makes this operation automatic. It scans the FM range, recognizes stations and automatically tunes into the frequency offering the best reception at any given time.

A further capability of the RDS is multilingual broadcasting. It will not be long before the Spanish truck driver on his way to deliver oranges to Lapland will be able to listen to traffic announcements in his own language, the message in Finnish being translated into his own language by a synthetic voice.

The European Commission is also studying the possibility of equipping car radios with a small computer fitted with a decoder to enable the driver to identify himself and indicate his position on the road. Thus, he would only receive traffic information of relevance to him or even personal messages such as "you are urgently requested to call your office (or home)". However, this project is still rather futuristic.

A European idea

Today, the RDS is to FM what the introduction of FM was as a solution to congestion in the AM bands of yesteryear. The RDS is a primarily European idea, since it is Europe that suffers most severely from the problem of frequency congestion.

Three official bodies have had a hand in the development of the RDS:

- the European Broadcasting Union (EBU) which, in March 1984, laid down specifications, and in March 1987 established the protocols for definition of transmissions and other frequencies;
- the International Radio Consultative Committe (CCIR) which, in 1986, adopted Recommendations on use of the system;
- the European Committee for Electrotechnical Standardization (CENELEC) which, in 1987, defined basic receiver characteristics.

After a long period of development, dating back to 1974, the various European countries have reached different stages of implementation of RDS projects or tests and trials. Several European countries have begun to introduce some of the different services offered by the RDS, including Austria, France (Télévision de France, TDF, inaugurated the first French RDS service in the France Inter network), the Federal Republic of Germany, Ireland, Sweden, Great Britain (in 1982 the BBC was the first broadcaster to use RDS transmissions on an experimental basis), Belgium, Denmark, Italy and Yugoslavia. These countries are to be joined by Norway, Portugal and Switzerland within the next few months.

Twenty European, Japanese and American manufacturers have developed prototype receivers for cars, for which the RDS concept was initially intended, as well as a number of receivers designed for the home.

Receivers have been on sale for only two years (Volvo was the first company to put them on the market) and do not yet all offer the whole range of potential facilities. They are still relatively expensive (around £400). It is anticipated that in the long term most car radios will be equipped with RDS and that the additional cost of the necessary equipment will be brought down to negligible levels.

For the time being, RDS is planned only for FM, although research is underway in the Federal Republic of Germany with a view to applying it also to AM.

What about North America?

Following in the footsteps of Europe, which stands at the forefront of the project, the United States have now entered the race, while the Canada Broadcasting Company (CBC) recently began experiments in Toronto.

Initially, the potential of RDS capabilities was not fully appreciated in the USA, where the usefulness of the system was questioned. Nevertheless, the USA is also afflicted by the problem of radio congestion, particularly in large towns.

The commercial side is also an important factor. A transmission using more than one frequency offers significant advertising potential for the American broadcaster, who will be able to extend his coverage area and secure regular listeners thanks to the PI system, for example. This will increase his income from advertising, which depends among other things on audience ratings.

In addition, the introduction of RDS on the North American continent would bring down significantly the unit cost of radio sets equipped with the system.

What is DAB?

DAB, or Digital Audio Broadcasting, is a precious innovation that will soon provide us with a sound quality equivalent to that of a compact disc, not only from satellite broadcasting, for which the new technique was originally intended, but also from terrestrial networks.

A pilot experiment was conducted two years ago by the EBU on the roads in Geneva. With a transmitter installed on Mount Salève and two radios in two cars driving around the town, the experiment produced extremely conclusive results in terms of sound quality. One advantage of digital transmission is that it is insensitive to spurious noise or parasites: the decoder recognizes only the wanted signal and nothing else. DAB could thus help to clean up the FM band by eliminating the effects of unwanted interference.

However, for the moment DAB is still at the planning stage. The equipment used in the pilot experiment in Geneva was much too voluminous and would have to be miniaturized before being launched on the market.

Another factor that makes DAB a thing of the more distant future is that, with the current state of technology, its introduction would necessitate the replacement of all radio receivers currently in use. At present, this represents a prohibitive investment.

However, we will not have to wait that long because Digital Audio Tape (DAT) is to be introduced within the next few months. DAT cassettes will offer a quality comparable to a compact disc, thereby already significantly improving recording and reception quality.

ELECTRONICS SCENE

SHARPER PICTURES IN THE AIR

A way of broadcasting high-quality cinema-type pictures over existing television frequencies has been unveiled by researchers at the BBC.

Their technique is said to give high-definition television pictures four times as sharp as current ones with enhanced colour and stereo sound. Called digitally assisted television, DATV, it takes the high-definition picture and selects parts of its electronic information.

Conventional TV pictures in the UK are transmitted at 1/50th second intervals. As the DATV signal contains four times as much information, it needs to be reduced by three quarters to fit the existing transmission system.

The DATV technique isolates static parts of the picture and stores them in the set, sending fresh information on them only one in four times. Similarly, it determines the direction and speed of movement in moving parts of the image, so that they too can be stored and sent four times less frequently.

WORLD INFORMATION SERVICE ON ARTIFICIAL INTELLIGENCE

One of the world's most comprehensive databases on artificial intelligence and related topics, located at the Turing Institute in Glasgow, is now available to all countries. Anyone with access to a computer terminal connected to a telephone line will be able to search the institute's database, which contains more than 50 000 references, with abstracts, to articles in journals, research reports, conference proceedings and books.

The institute has previously made its database available to the dozen or so companies that are its affiliate members in Europe. Now, it has teamed up with Data-Star, based in Switzerland, which claims to be Europe's leading on-line database 'host'. Databases held by Data-Star can be accessed by terminals on a world-wide basis.

At Glasgow, the AI database is updated daily. A new tape is sent to Data-Star every month to provide what is said to be an unrivalled source of the latest information on research applications and market trends in such matters as expert and knowledge-based systems, machine learning, pattern recognition, advanced robotics, neural networks, software and many other aspects of AI.

Maintaining contact with research institutes around the world, the Turing Institute at present holds some 16 000 articles from about 180 journals; a similar number of papers from major conferences and workshop meetings; 9000 reports from about 200 research institutes throughout the world, and a further 9000 monographs, textbooks and collected works.

PRIVATE MOBILE RADIOS IN EUROPE

A report from Frost & Sullivan* predicts that Public Access Mobile Radio (PAMR) services in Europe will grow explosively as Private Mobile Radio (PMR) equipment sales begin to decline.

PAMR is defined as a non-cellular public subscription trunked telecommunications service that may offer access to the public telephone network.

Britain is the largest PAMR market and will remain so well into the 1990s. The report assumes that neither Federal Germany nor Italy will begin PAMR for quite a few years yet and that France will not upgrade its old-style system.

**PRIVATE MOBILE RADIOS IN EUROPE* (#E1130), available from Frost & Sullivan, Sullivan House, 4 Grosvenor Gardens, LONDON SW1W 0DH, telephone 01-730 3438.

SINGLE EUROPEAN MARKET FOR TELECOMMUNICATIONS

By 1992 the European Community will have a single market for telecommunications equipment, with a broadly and consistently deregulated telecoms service environment designed to promote competition rather than protect national interests. As such, it presents an enormous challenge to all of the EC's telecoms players, and perhaps none more so than those in the United Kingdom.

In terms of equipment manufacturing, the UK has not yet made the impact it deserves to. Its intra-EC telecoms trade deficit is exceeded only by Italy.

There are good historical reasons for Britain's lack of penetration of European markets. Apart from the fact that these markets have, until now, been highly protected to the benefit of domestic suppliers, British companies have traditionally looked further afield for export opportunities. The European Commission may successfully break down protectionism, but it can not rip out the established distribution and trading networks overnight. Nor can British companies buy their way into EC markets by acquiring local distributors and manufacturers, since most of the distribution networks are dominated by giants like Siemens and Alcatel.

Instead, the British will have to concentrate on emerging markets, where there are no established leaders – such as in the emerging mobile equipment arena – or else seek joint venture agreements with established market leaders.

TRANSPUTER 'COMPUTER' BREAKTHROUGH

A breakthrough in achieving the high levels of computer power required for many digital signal processing applications has been announced by Marconi Radar Systems.

Incorporating the multiprocessing power of the INMOS transputer, the S7400 transputer array signal processor was developed by the company initially to service the demanding requirements of modern radar signal processing. The – up to now – prohibitively high cost of array processors had forced manufacturers to build signal processing systems with dedicated hardware. This approach lacks flexibility and requires a long design and manufacturing cycle.

The transputer is a fully software-programmable device that has inherent advantages over other technologies – such as ASIC-based processors – in that it is totally uncommitted, so offering users great flexibility with a standard hardware and foundation software package.

MINI EPROM PROGRAMMER

J. Ruffell

Many constructors have good reasons for preferring a low-cost EPROM programmer with manual data and address to a full-blown programmer operating under computer control. First, they may not have a computer; second, they do not mind spending some time on programming small amounts of data; and third, they object to the expenditure on an instrument that is only occasionally called upon.

The programmer is definitely not intended for loading huge amounts of data into EPROMs. Even if you could manage to program bytes faultlessly at a rate of one per second, it would take more than 18 hours to load all 65,536 bytes (64 Kbytes) in a Type 27512 EPROM, the largest the present programmer can handle. Moreover, it is a common misunderstanding to associate EPROMs with microcomputer systems that require large amounts of data. As has been shown in a number of projects in this magazine over the past few months, there are quite a few occasions where no more than, say, 256 or 512 bytes are involved, such as where EPROMs function as programmable look-up or conversion tables.

Although the circuit diagram of the mini EPROM programmer (Fig. 1) looks crowded, it should be noted that most components go into the power supply to ensure that the high programming voltage is not applied to the EPROM until the 5 V supply voltage is present — the reverse sequence would have disastrous consequences. Also note that an EPROM must never be removed from the working programmer, because the order in which the programming voltage and the supply voltage are removed might just be wrong.

How it works

Although the supply circuit already looks quite crowded in places, it is not complete without an external regulated power supply to furnish the programming voltage plus about 750 mV. The input voltage to the circuit may be adjusted by measuring the programming voltage at point Pv. The programming voltage is determined by the EPROM type and its manufacturer. Regulator IC$_3$ reduces the programming voltage to 5 V which is used to power the EPROM and the programmer circuit. Transistor T$_1$ prevents the programming voltage being applied to the EPROM before the 5 V supply voltage. The transistor is controlled by a monostable multivibrator (MMV), IC$_{1a}$. After this has been triggered, its Q output remains high until it is reset via its $\overline{\text{CLR}}$ input. This input is connected to the rest of the circuit in a manner to ensure that IC$_{1a}$ is reset if the +5 V supply voltage disappears, or when there is no supply voltage at all. The latter condition may appear superfluous, but the programming voltage is immediately disconnected from the relevant EPROM pin when the programmer is switched off with S$_1$. The 5 V supply voltage, however, remains present for a short while because the electrolytic capacitors take some time to discharge. Conversely, IC$_{1a}$ can not be set until the +5 V supply voltage is present. The SET input of the MMV is formed by trigger input B, which is connected to network R$_3$-C$_5$. The voltage on C$_5$ takes a few seconds to rise to a level that enables IC$_{1a}$ to be set, and, consequently, the programming voltage to be applied to the EPROM. Capacitor C$_{10}$ is required only if the $\overline{\text{CLR}}$ input of IC$_{1a}$ is erroneously actuated by input voltage fluctuations. The value of C$_{10}$ should be between 100 pF and 10 nF and must be determined empirically. In general, the capacitor must be kept as small as possible.

Bi-colour LED D$_7$ indicates the status of the EPROM programmer. The LED turns red (T$_3$ off; T$_4$ on) if the 5 V supply voltage is present, and green if both the 5 V and the programming voltage are present.

The circuit around IC$_{1b}$ (also a MMV) is a programming pulse generator. When S$_2$ is actuated, a single 50-ms programming pulse is generated. An intelligent programming algorithm with variable programming pulse length is, of course, not feasible in a simple circuit like this. Even if it were available, the total programming time would not be reduced because the data and addresses are set manually, which takes much longer than 50 ms in any case.

The bulk of the signals in the programmer circuit emanates from DIP switches and associated pull-up resistors. Addresses are set with S$_4$ and S$_5$, data with S$_6$. Switch S$_3$ is used to select the EPROM type. The connections it makes are in ac-

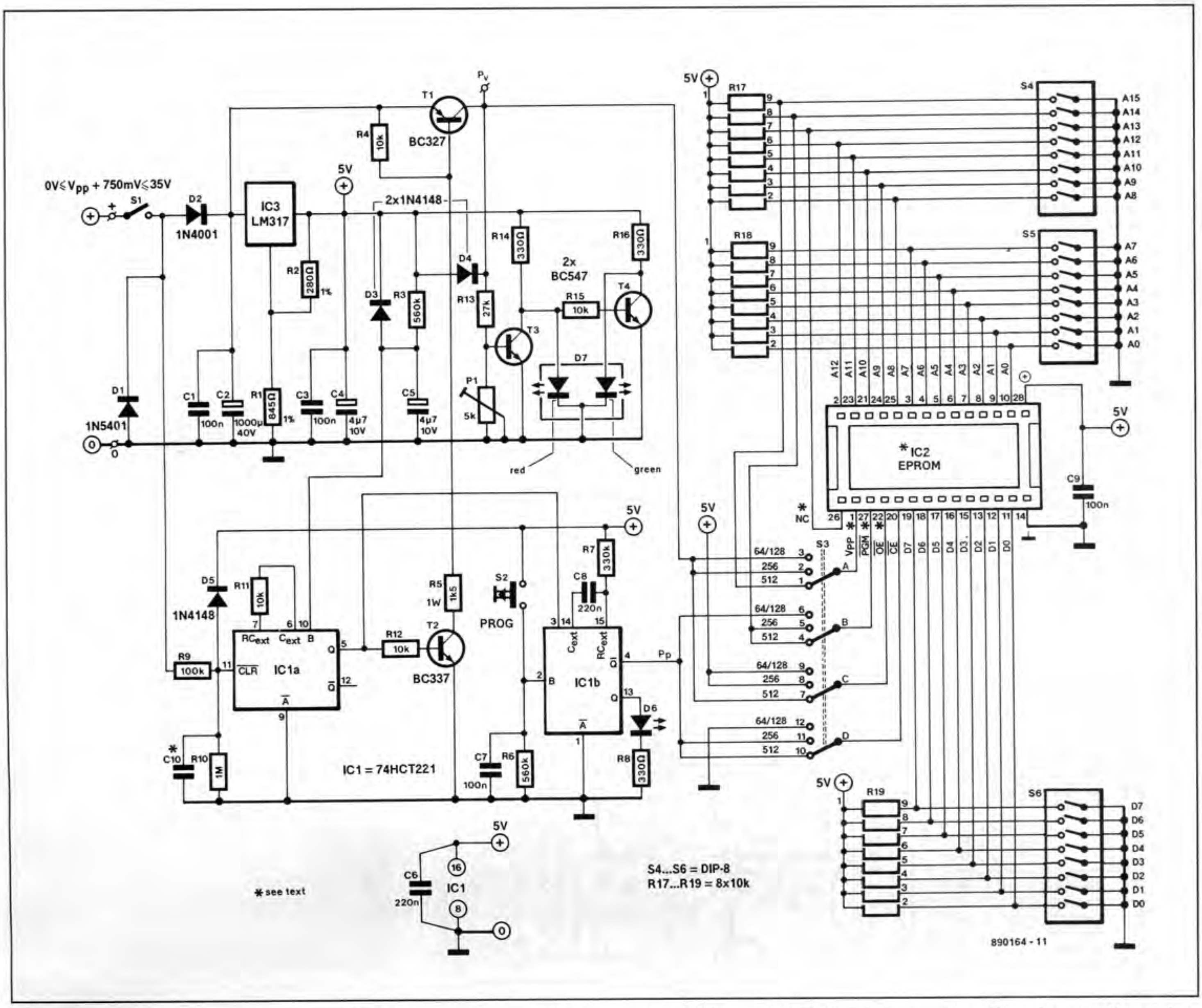


Fig. 1. Circuit diagram of the budget EPROM programmer, the larger part of which consists of the power supply with automatic Vpp delay.

cordance with the EPROM data listed in Table 1.

Construction

The printed-circuit board for the programmer is shown in Fig. 3. Start the construction by fitting the wire links. Next, fit the resistors and capacitors. Each of the three single-in-line (SIL) resistor arrays may be replaced by eight vertically mounted, discrete resistors whose upper terminals are cut short and commoned by a horizontal wire that goes into the hole provided for the +5 V connection of the array.

The semiconductors are fitted next, with the exception of the LEDs. IC3 does not need a heat-sink, and is bolted straight on to the PCB. Mount rotary switch S3, but do not cut its spindle as yet.

Be sure to mount the components that protrude from the front panel at the correct height above the board. This involves the LEDs, on/off switch S1, programming switch S2, the data/address DIP switches and the ZIF (zero-insertion force) socket

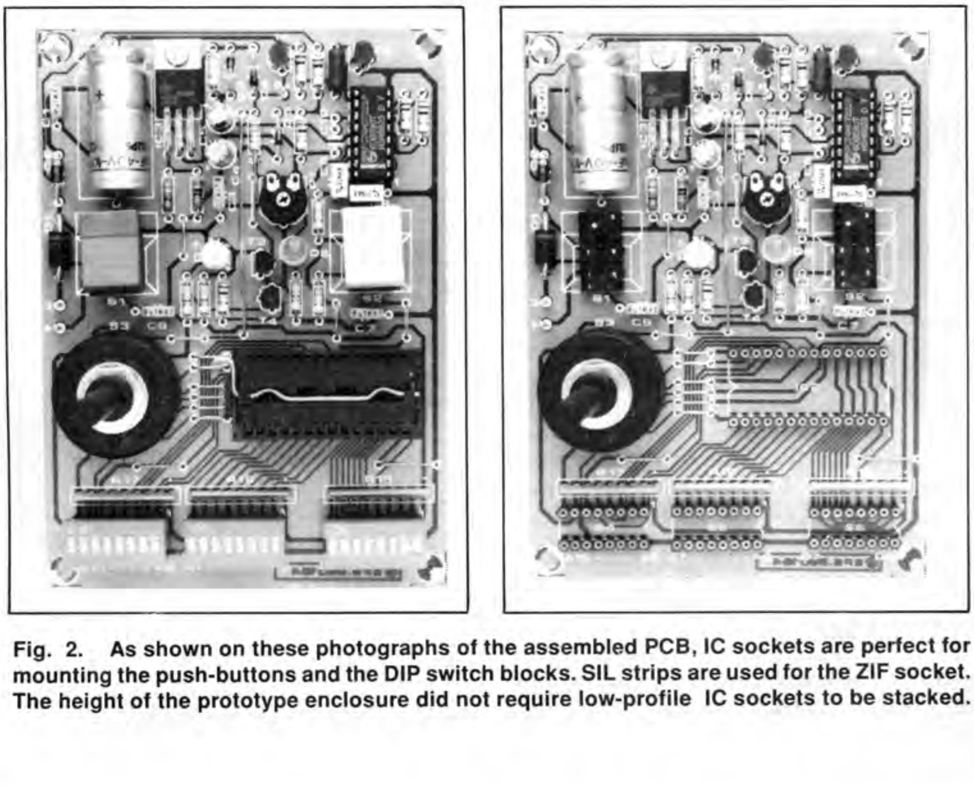


Fig. 2. As shown on these photographs of the assembled PCB, IC sockets are perfect for mounting the push-buttons and the DIP switch blocks. SIL strips are used for the ZIF socket. The height of the prototype enclosure did not require low-profile IC sockets to be stacked.

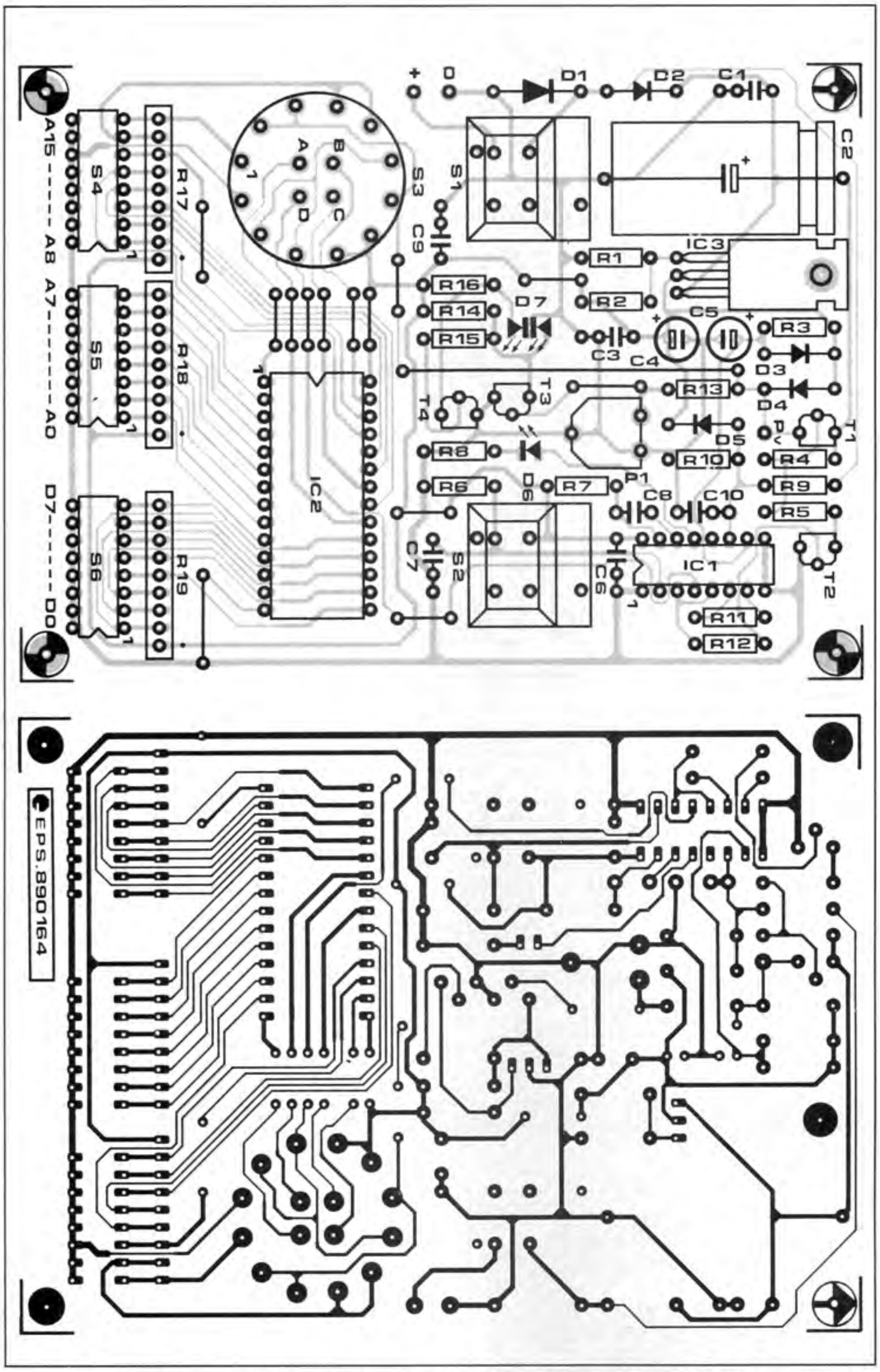


Fig. 3. Track layout and component mounting plan of the single-sided PCB for the mini EPROM programmer. Start the construction with fitting the wire links.

Parts list

Resistors:
R_1 = 845Ω; 1%
R_2 = 280Ω; 1%
R_3;R_6 = 560k
R_4;R_{11};R_{12} = 10k
R_5 = 1k5; 1 W
R_7 = 330k
R_8;R_{14};R_{16} = 330Ω
R_9 = 100k
R_{10} = 1M0
R_{13} = 27k
R_{15} = 10k
R_{17};R_{18};R_{19} = 8-resistor; 9-pin SIL resistor array 10k
P_1 = 5k preset H

Capacitors:
C_1;C_3;C_7;C_9 = 100n
C_2 = 1000µ; 40 V
C_4;C_5 = 4µ7; 10 V; radial
C_6;C_8 = 220n

Semiconductors:
D_1 = 1N5401
D_2 = 1N4001
D_3;D_4;D_5 = 1N4148
D_6 = LED
D_7 = 3-terminal bi-colour LED
T_1 = BC327
T_2 = BC337
T_3;T_4 = BC547
IC_1 = 74HCT221
IC_2 = EPROM to be programmed
IC_3 = LM317

Miscellaneous:
S_1 = self-locking push-button; ITW Type 61-20204000 $^+$.
S_2 = momentary action push-button; ITW Type 61-10204000 $^+$.
S_3 = PCB-mount 4-pole 3-way rotary switch.
S_4;S_5;S_6 = 8-way DIP switch block.
28-way IC socket (ZIF type preferred).
PCB Type 890164 (see Readers Services page).

We regret that the front-panel foil for this project is not available ready-made.

$^+$ ITW Switches • Division of ITW Ltd. • Norway Road • Hilsea • PORTSMOUTH PO3 5HT. Telephone: (0705) 694971.

for the EPROM. A good way of achieving the correct height for the DIP switches is to use wire-wrap sockets or simply three or four stacked low-profile IC sockets (see Fig. 2). Much depends on the enclosure used.

Figure 4 shows a suggested lay-out for the front panel of the programmer. Make a photocopy of this drawing and use it as a template to cut and drill the metal or ABS front-panel of your enclosure.

Setting up

Connect the external power supply and adjust it to an output that results in +10.0 V at point Pv (you may have to wait

Pin	2764	27128	27256	27512
1	Vpp	Vpp	Vpp	A15
22	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$/Vpp
26	n.c.	A13	A13	A13
27	PGM	PGM	A14	A14

Signal	2764	27128	27256	27512
$\overline{\text{OE}}$	H	H	H	
$\overline{\text{OE}}$/Vpp				Pv
Vpp	Pv	Pv	Pv	
$\overline{\text{CE}}$	L	L	⊔	⊔
$\overline{\text{PGM}}$	⊔	⊔		

Table 1. EPROM programming data as set by the EPROM type switch on the front panel.

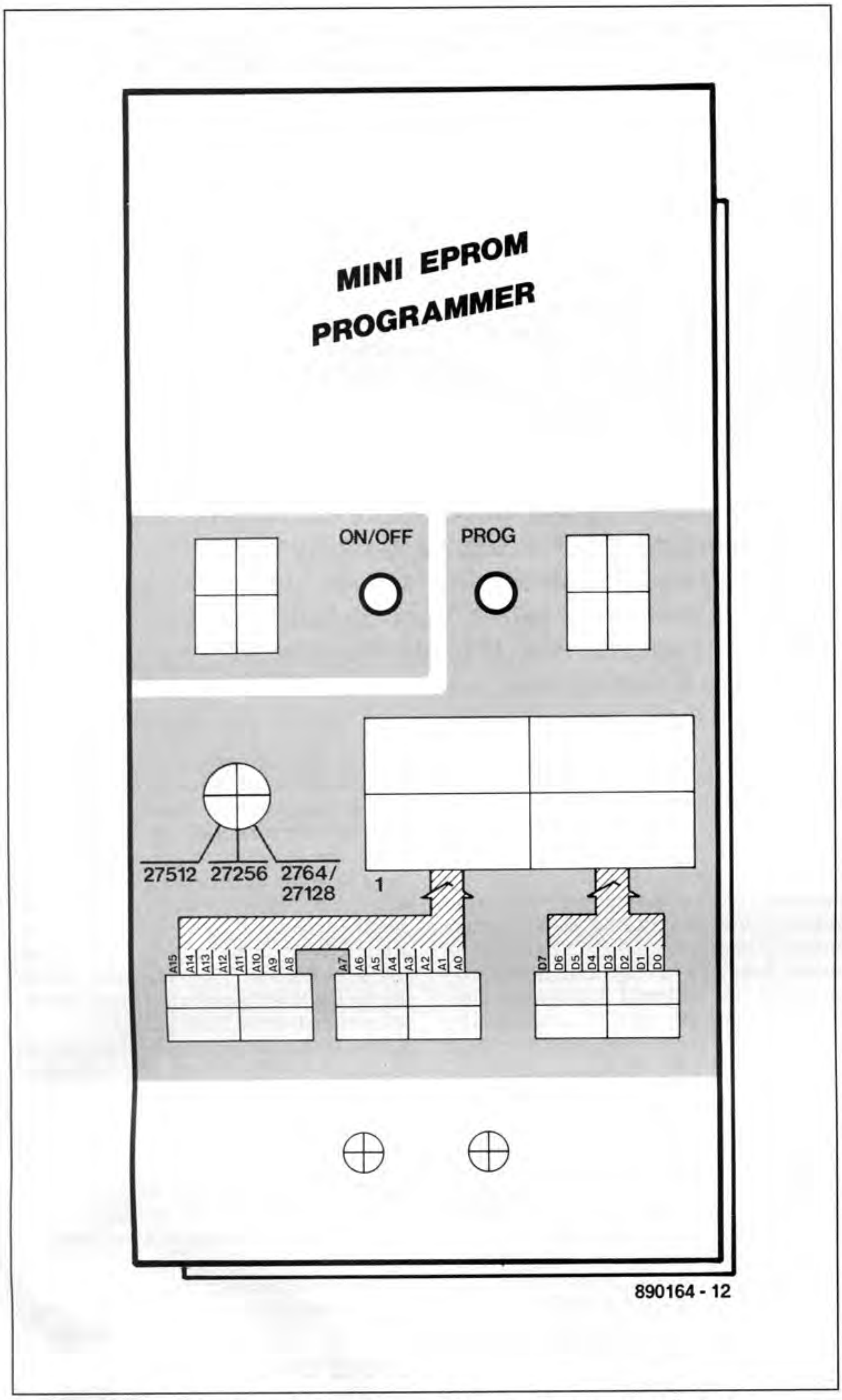


Fig. 4. **Suggested front-panel layout shown at true size for easy reproduction.**

a second or two until T_1 is turned on). Adjust P_1 until the status LED changes colour. This completes the adjustment procedure.

Do's and don'ts

There are a few basic rules to keep in mind when using the mini EPROM programmer:

- Before inserting an EPROM, always check the programming voltage at point Pv and adjust your power supply to set the correct value for the device to be programmed. Next, set the EPROM type on S_3.
- Never insert or remove an EPROM with the programmer switched on.
- And, finally, *think* before actuating the programming switch!

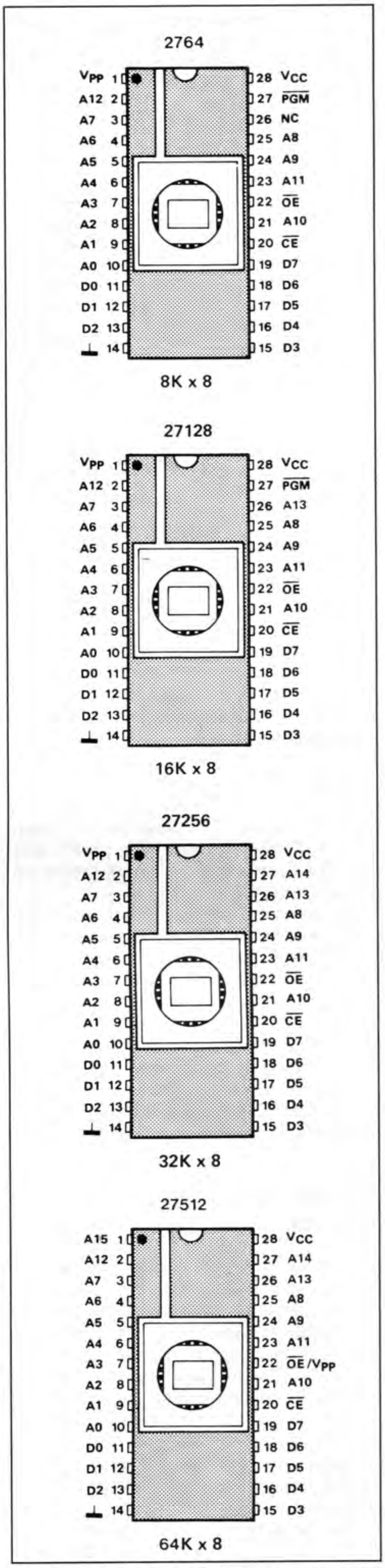


Fig. 5. **Pin-outs of the four members of the 27xxx family that can be programmed.**

TELEPHONE ANSWERING UNIT

This automatical telephone answering unit, designed by ELV GmbH, uses a 256-Kbit voice recording circuit to store and replay your spoken message of up to 15 seconds. Noteworthy features are that it is available as a complete kit, provides a battery back-up facility, and does not require alignment. No provision is made, however, to record incoming calls.

From the onset, it should be made clear that the telephone answering unit is not type-approved by British Telecom, and may not be connected to the public switched telephone network (PSTN). This limits its use to domestic and office telephone exchanges. In countries other than the UK, the relevant PTT authorities should be contacted for information on type approval.

A digital sound processing circuit in the telephone answering unit does away with the need of the more usual cassette or tape recorder to replay the recorded message. Apart from its four front-panel mounted controls, the unit has no parts or controls subject to mechanical wear and tear.

The unit is of the direct-coupled type, i.e., it does not use a costly transformer that complicates the line interface circuit and limits the speech bandwidth.

Simple to connect and operate

The telephone answering unit is simply connected in parallel with the line terminals inside an existing telephone set. In most European countries, the telephone line connections are marked 'a' and 'b', or 'LA' and 'LB'. Although terminals 'a' and 'b' have the corresponding indications on the printed-circuit board, the connections between the line and the telephone answering unit may be reversed without causing damage because the input of the circuit uses a bridge rectifier.

The unit is powered by an inexpensive mains adaptor with an unregulated output voltage of 12 VDC at 100 mA.

The on/off switches and the associated indicator LED are located at the left of the front panel. The unit is switched on and off by briefly pressing the relevant button.

The LED lights at normal intensity if the unregulated input voltage supplied by the mains adaptor is between 12 V and 15 V. A 9 V rechargeable battery inside the enclosure ensures that the answering unit remains operative during mains voltage interruptions. The 'on' LED lights at reduced intensity if the unit is battery-powered. An internal voltage monitor ensures that the unit is automatically switched off when the battery voltage drops below 7.5 V. When the mains voltage is switched on again, the battery is recharged, but the answering unit is not switched on automatically because the speech content of its internal RAM is erased or corrupted. The unit can be taken into operation again only by switching it on with the front panel control.

To record a message, press the RECORD button briefly. The associated LED lights. Wait one or two seconds before delivering the message via the built-in condenser microphone located between the RECORD key and the LED. Speak at a distance of about 20 cm to 50 cm from the microphone. An internal amplifier with level-dependent gain ensures the best drive margin for the speech digitizer.

There is no technical reason for the short pause before the message, but callers may be unable to hear the first two or three words of the message because of the connection noise that is often heard immediately after a call is answered.

The telephone answering unit has an outgoing message length of 15 seconds. This may appear relatively short, but in reality allows a message of reasonable duration to be recorded without having to speak too quickly.

The LED at the centre of the front panel lights when the recorded message is transmitted. This happens automatically when the unit answers the call, or manually when the START button is pressed. Although the message can be heard by picking up the receiver of the parallel-connected telephone set, the line driver circuit in the answering unit can not be overridden by the normal speech signal. The line circuit eliminates virtually any external signal that resembles line unbalance or noise. This means that you can not hear the calling party, while the calling party hears the answer message only.

The recorded message may be interrupted while it is transmitted by pressing the OFF key. It should be noted, however, that this also clears the message.

A new message may be recorded as often as required by pressing the RECORD key. The previous message is automatically cleared to make the practical use of the answering unit as simple as possible.

Circuit description

The circuit diagram in Fig. 1 shows that the AF signal supplied by the electret microphone is applied to the –input (pin 6) of opamp OP1 via coupling capacitor C_7. The gain of the opamp is determined by feedback resistor R_{11}. The amplified microphone signal at pin 7 is applied to the comparator input, pin 29, of the voice recorder chip, IC_1.

The signal conversion and storage circuit works on the basis of adaptive delta modulation (ADM). In this process, a comparator is used to determine whether the instantaneous level of an analogue input signal is above or below that of the reference level established by summation

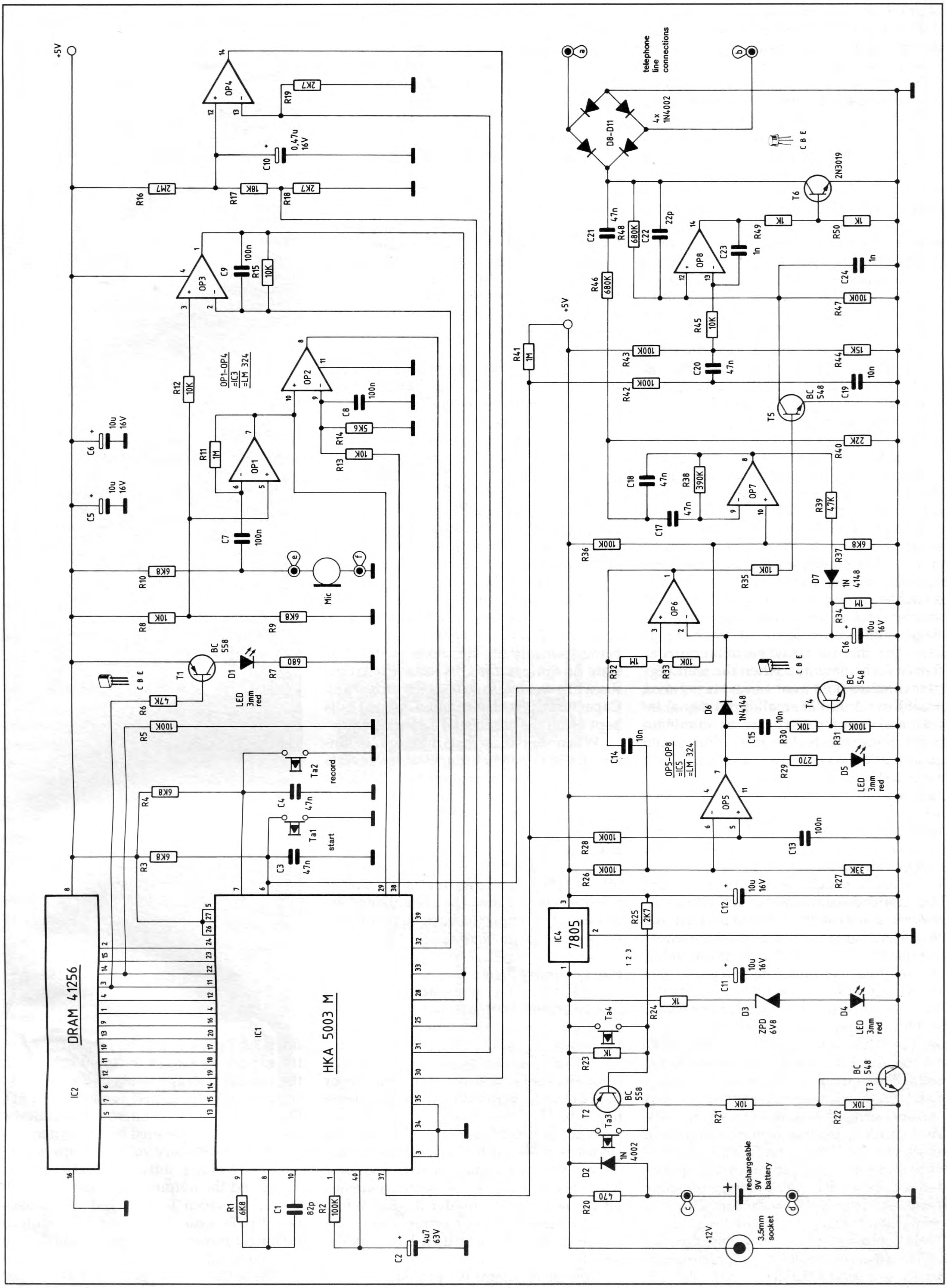


Fig. 1. Circuit diagram of the telephone answering unit. The answer message is recorded and stored digitally in 256-kbit RAM chip IC2.

of previously taken samples. The result of the comparison is a 0 or a 1 which is stored into the memory. The next step involves a further comparison between the current input level and the new (*adaptively* established) reference level. The result is another 0 or 1 which goes into the memory.

The digital-to-analogue conversion is essentially the reverse process, and is based on current-controlled integration of the digital memory data. The content of the memory is fed out sequentially. Any 1 or 0 causes the current output amplitude to become greater or smaller respectively.

The Type HKA5003M integrated circuit requires only four external opamps and a handful of passive components to handle the D-A and A-D conversions, as well as the memory addressing. Unfortunately, the scope of this article does not allow a closer analysis of the internal operation of the HKA5003M to be given, so that it has to be treated like a black box.

Random-access memory (RAM) chip IC_2 has capacity for storing up to 262,144 bits (0s or 1s). At a maximum speech recording time of 15 s, this results in a data rate of 17,476 bits per second, which corresponds to 'almost' six bits for an AF input frequency of 3,000 Hz. Since this 'digital resolution' is too low to ensure acceptable quality of the digitized speech signal, the dynamic response of IC_1 is boosted. This is achieved with an internal current source which is composed of quantization stages, and controlled by a 4-bit shift register. The quantization level of the current source is incremented when the shift register contains only 0s or 1s, and is reduced to almost nought at small input signal levels and low frequencies to eliminate background noise. The operation of the quantization stages is not unlike that of a compander, and ensures acceptable playback quality for signals up to 3,000 Hz, i.e, for most components in the frequency spectrum of speech.

Answer circuit

The speech processor chip has an onboard refresh controller which allows an inexpensive dynamic RAM to be used. All 262,144 bits are read sequentially to transmit the 15-s message. The serial signal at pin 37 of IC_1 is applied to integrator C_{19} via R_{42}. Coupling capacitor C_{20} feeds the filtered signal to the output driver formed by OP_8, T_6 and associated parts. Output pin 14 of OP_8 is connected to the base of T_6 via R_{29} and R_{50}. This causes the collector voltage of T_6 to take a value that results in equal voltages at the inverting (–) and non-inverting (+) inputs of opamp OP_8. The –input is held at a reference voltage of about +0.6 V by potential divider R_{43}-R_{44}. With the amplification of the opamp determined by R_{47}-R_{48}, a voltage of about 5 V is obtained at the collector of T_6, but only when the unit is actuated, i.e., effectively connected to the telephone line.

The reference voltage at junction R_{43}-R_{44}-R_{45}-C_{20} is modulated with the digitized speech signal. As a result, this is superimposed on to the collector voltage of T_6, and from there, on to the telephone line.

The above situation applies to the 'playback' mode only, i.e., when the unit is answering a call. Otherwise, T_5 is turned on, so that the +input of OP_8 is at a lower potential than the –input. As a result, opamp output pin 8 is at virtually 0 V, keeping T_6 disabled. The telephone line terminals (a and b) are at 50 V to 60 V.

Receive circuit

When the extension is called, components C_{21} and R_{46} feed ring signals on the line to a bandfilter around OP_7. The alternating output voltage of OP_7 is rectified by R_{39}-D_7 and applied to combination C_{16}-R_{34}. After a few ring pulses, the voltage on C_{16} exceeds that at the +input of OP_6, which consequently toggles. The resultant low level at the output of the opamp causes T_5 to be turned off via R_{35}. This, in turn, causes the output stage to be enabled via pin 12 of OP_8. The output transistor, T_6, is driven to a level where its collector is at about 5 V. This enables the telephone exchange to detect that the call is being answered.

Next, C_{14} causes OP_5 to toggle and supply a high level at its output. The resultant pulse from C_{15}-R_{30} is applied to the base of T_4, whose collector voltage drops briefly. The START input of IC_1, pin 6, is taken low. The output voltage at pin 37 of the speech synthesizer rises from 0.5 V to about 2.0 V when the answer message is being transmitted. This level enables the state of comparator OP_5 to be frozen via R_{28} while the message lasts (approx. 15 s). Capacitor C_{16} is also charged, so that T_5 is kept off in the absence of a ring signal.

When the recorded message is finished, the voltage at pin 37 of IC_1 reverts to 0.5 V, so that the output of OP_5 goes low, and C_{16} is slowly discharged. When the voltage on C_{16} drops below the reference voltage of OP_6, the opamp toggles and supplies a high level at its output. As a result, T_5 is turned on, and T_6 is turned off via OP_8 so that the answering unit is disconnected from the telephone exchange. It is connected back again by ring pulses as explained above.

Power supply

In most cases, the mains adaptor is only lightly loaded, so that its output voltage is between 13 V and 15 V. The 9 V battery in the answering unit is charged via R_2.

Power indicator D_4 passes the current through series resistor R_{24} and zener diode D_3, and lights at its nominal intensity.

When button Ta_3 (ON) is pressed, the circuit is powered by T_3, which is turned on via R_{21}. The voltage across regulator IC_4 is about 9 V (14 – 5), which switches on T_2 via potential divider R_{23}-R_{25}. When Ta_3 is released, the circuit remains on by virtue of R_{23} which feeds a base current into T_3.

Voltage regulator IC_4 provides the 5 V supply voltage for the entire circuit. When the mains voltage disappears, D_2 conducts, so that the 9 V battery takes over the supply. Although the input voltage of the regulator drops to about 8 V, the circuit remains on because T_2 conducts. LED D_4 lights at reduced intensity to indicate that the unit is powered by the battery.

Parts list

Resistors:
R_{29} = 270Ω
R_{20} = 470Ω
R_7 = 680Ω
R_{23};R_{24};R_{49};R_{50} = 1k0
R_{18};R_{19};R_{25} = 2k7
R_{14} = 5k6
R_1;R_3;R_4;R_9;R_{10};R_{37} = 6k8
R_8;R_{12};R_{13};R_{15};R_{21};R_{22};R_{30};R_{33};
R_{35};R_{45} = 10k
R_{44} = 15k
R_{17} = 18k
R_{40} = 22k
R_{27} = 33k
R_6;R_{39} = 47k
R_2;R_5;R_{26};R_{28};R_{31};R_{36};R_{42};R_{43};
R_{47} = 100k
R_{38} = 390k
R_{46};R_{48} = 680k
R_{11};R_{32};R_{34};R_{41} = 1M0
R_{16} = 2M7

Capacitors:
C_{22} = 22p
C_1 = 82p
C_{23};C_{24} = 1n0
C_{14};C_{15};C_{19} = 10n
C_3;C_4;C_{17};C_{18};C_{20};C_{21} = 47n
C_7;C_8;C_9;C_{13} = 100n
C_{10} = 0.47µ; 16 V
C_2 = 4.7µ; 63 V
C_5;C_6;C_{11};C_{12};C_{16} = 10µ; 16 V

Semiconductors:
IC_3;IC_5 = LM324
IC_1 = HKA5003M
IC_4 = 7805
IC_2 = 41256
T_3;T_4;T_5 = BC547B
T_1;T_2 = BC558
T_6 = 2N3019
D_8 – D_{11} = 1N4002
D_2;D_6;D_7 = 1N4148
D_3 = ZPD6V8
D_1;D_4;D_5 = LED; 3 mm; red

Miscellaneous:
Ta_1 – Ta_4 = PCB-mount push-button.
Qty 1: Condenser microphone.
Qty 1: PP3 battery clip.
QTY 1: 3.5 mm dia. supply socket.
Qty 6: solder pin.
10 cm light-duty wire.
20 cm 2-way flexible cable.

When the battery voltage drops below 8 V, the voltage difference between the input and the output of IC_4 also drops to a level at which T_2 is turned off. Consequently, T_3 is turned off, and the circuit is no longer powered. The power indication LED goes out.

The battery is charged again as soon as the mains voltage is restored, but the telephone answering unit remains off until

Ta$_3$ (ON) is actuated. In most cases, a new message must be recorded only if the answering unit has completely run out of battery power at some time. Fortunately, this should not be required too often since the capacity of the 9 V battery supplied with the kit is such that most power cuts can be coped with.

Length of the message

It will be clear that the time available for the message is inversely related to the rate at which it is recorded and reproduced. The output frequency of the clock oscillator on board IC$_1$ may be changed to individual requirements to achieve a message duration other than 15 seconds as determined by parts R$_1$ and C$_1$. The resistor may be changed within a range of 3.3 kΩ to 15 kΩ, with the lower value resulting in improved speech quality at a short message duration.

Construction

The printed-circuit boards for the telephone answering unit are shown in Fig. 2. Start the construction by fitting the 17 wire links and all the passive parts. Next, fit the semiconductors. The size and dimensions of the boards are geared to the ABS enclosure supplied with the kit.

On their completion, the boards are carefully examined with reference to the parts list and the component overlay. Next, position the keyboard PCB vertically against the front edge of the main PCB. The lower edge of the keyboard PCB must protrude at about 1.5 mm below the track side of the main PCB. Align facing solder tracks and join each pair which a little solder, taking good care not to cause short-circuits.

Fit the 3.5 mm power supply socket into a hole in the rear panel and connect the two light-duty supply wires to the relevant terminals on the PCB. The connection to the telephone line is made direct via a short length of 2-way flexible cable.

The telephone answering unit requires no alignment, and is ready for use as soon as the PCBs and the batteries have been fitted into the case.

A complete kit of parts for the telephone answering unit is available from the designers' exclusive worldwide distributors (regrettably not in the USA and Canada):

ELV France
B.P. 40
F-57480 Sierck-les-Bains
FRANCE
Telephone: +33 82837213
Fax: +33 82838180

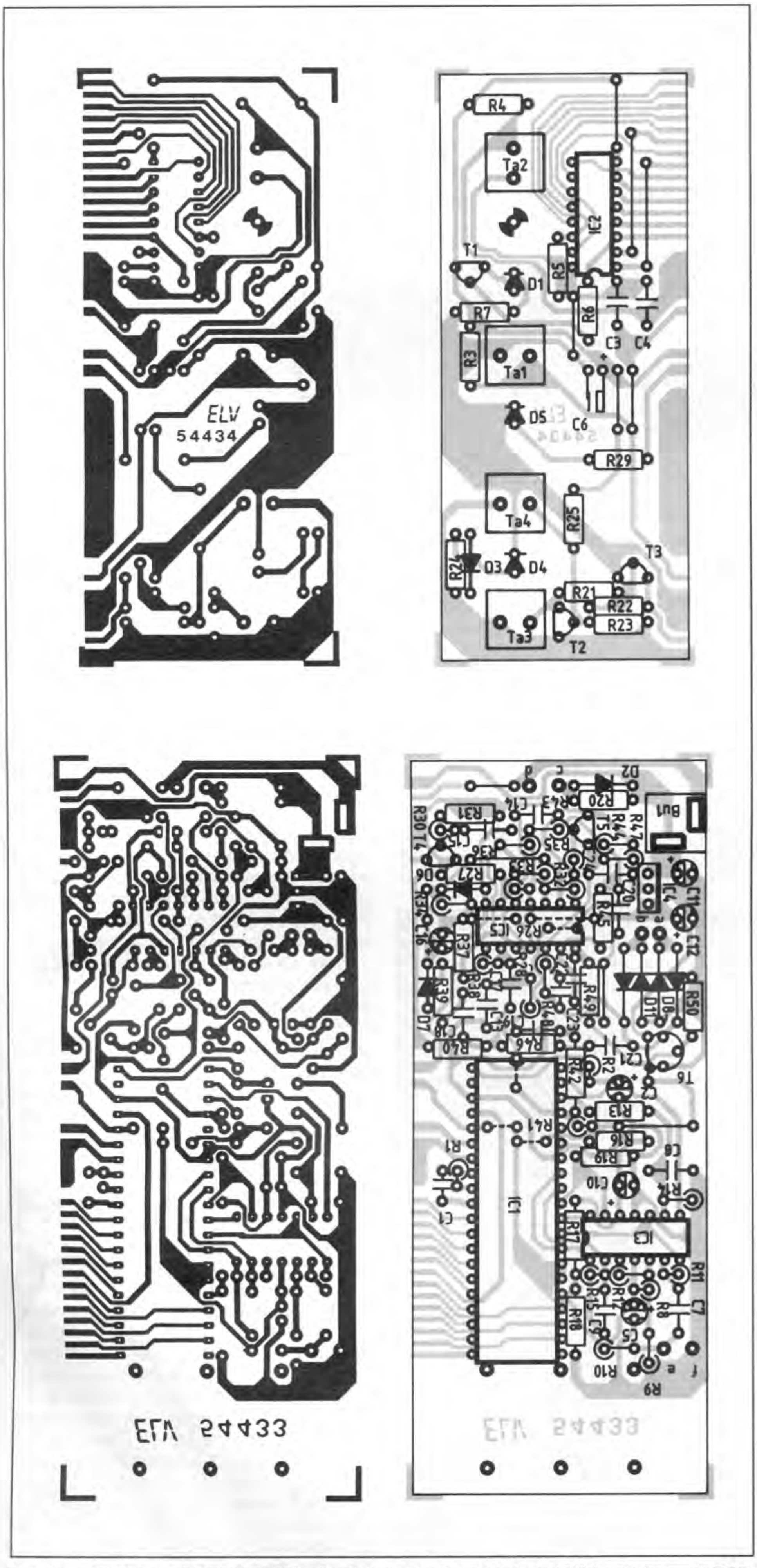


Fig. 2. Top views and component mounting plans of the keyboard PCB and the main PCB.

SIMPLE AC MILLIVOLTMETER

The third instrument in our series on budget test equipment is a wideband millivoltmeter with no fewer than twelve ranges, quite reasonable accuracy, a sensitivity of 200 µV and a frequency range from 20 Hz to over 2 MHz.

T. Giffard

A sensitive AC millivoltmeter is a useful instrument even if an oscilloscope is already available in your electronics workshop. This is mainly because signal levels are easier read from a meter scale than from an oscilloscope screen, which requires counting graticule divisions, multiplication by the set sensitivity, and conversion from the peak-to-peak value to the rms (root-mean-square) value. The AC millivoltmeter is also smaller and more sensitive than the average oscilloscope, and in addition may be powered by batteries. Compared to the digital multimeter, the AC millivoltmeter offers a much greater bandwidth. Although hard to beat for DC measurements, most DMMs have a frequency range of just 400 Hz which makes them really unsuitable even for signal tracing and frequency response measurements in AF amplifiers. By contrast, the AC millivoltmeter has a bandwidth of 20 Hz to 2 MHz.

The test instrument described here has no fewer than 12 measurement ranges from 0.2 mV to 60 V, and a high input impedance of 1 MΩ. The highest range, 60 V, allows output voltages of powerful AF amplifiers to be measured, while the most sensitive range, 0.2 mV, is suitable for direct signal level measurements on microphones and pick-up cartridges.

The choice of the enclosure and the design of the front-panel of the AC millivoltmeter are in line with the two earlier described instruments.

Circuit description

Since the instrument measures AC voltage only, off-set and drift are not normally problems in the amplifier stages. This means that integrated differential amplifiers in the form of operational amplifiers are not needed, and may be replaced by a circuit based on discrete transistors. The final version of this circuit was found to offer good stability at a reasonable bandwidth by virtue of the accurately compensated voltage divider at the input, and a PCB design that prevents problems with wiring capacitance by accommodating the range switch on the printed-circuit board.

SIMPLE AC MILLIVOLTMETER

AV measurement ranges:

0.2 mV; 2 mV; 20 mV; 200 mV; 2 V; 20 V
0.6 mV; 6 mV; 60 mV; 600 mV; 6 V; 60 V

Accuracy:

- approx. 5% at 2 MHz with selected compensation capacitors in input attenuator; approx 3% at 100 kHz (depending on meter error).
- approx. 2% at 15 kHz; 10% above 15 kHz with non-selected standard MKT capacitors in input attenuator.

Bandwidth (0.5 dB):

17 Hz to 2 MHz

Input impedance:

1 MΩ//10 pF

Battery voltage:

nominal:	9 VDC
maximum:	10 VDC
minimum:	7.5 VDC

Current consumption:

7.5 mA typ. at 9 V.

Voltage divider

The circuit diagram in Fig. 1 shows frequency compensation capacitors fitted in parallel with every resistor in the input attenuator around rotary switch S_1. These capacitors linearize the frequency response above 500 kHz. Ceramic capacitors are connected in parallel with larger MKT (metallized multi-layer theraphtelate) types as a fine correction to the compensation at relatively high frequencies. If possible, the ceramic capacitors are selected to give a time constant of 11 µs for each of the *R-C* combinations in the voltage divider.

Input amplifier

Depending on the position of S_2 in the measurement amplifier, the AC voltage at the gate of FET T_1 that results in full-scale deflection of the meter is either 0.2 mV or 0.6 mV. The gate of the FET forms a very high impedance so that the voltage divider is hardly loaded. Components D_1-D_2 and R_8 protect the gate against overvoltage. Diodes D_1 and D_2 conduct at gate voltages of about +9.6 V and −0.6 V respectively and afford protection to about 50 V in the 0.2 mV range. Capacitor C_{13} prevents R_8 and its associated stray capacitance (the FET, the diodes and the relevant PCB tracks) forming a low-pass filter that would limit the bandwidth of the millivoltmeter. It should be noted, however, that the reactance of C_{13} drops with increasing frequency, which reduces the protective effect of the diodes at frequencies above 40 kHz or so. The values of R_8 and C_{13} are, therefore, a compromise between bandwidth and protection over a reasonable frequency range.

FET T_1 is not included in the feedback circuit of the measurement amplifier that follows it. It has its own feedback resistor, R_{11}, to give an amplification of about 1.5 times. R_9 functions as a drain resistor for direct voltage only. For alternating voltages, it is decoupled by C_{15} and C_{16}. These parts decouple the supply voltage and so help to stabilize the sensitive input stage. The DC setting of the FET is determined by the source resistor: since the gate is effectively grounded by the resistor ladder network, the voltage drop across the source resistor creates a negative gate voltage (U_{GS}), which determines the current through the drain- and the source resistors. The resultant bias setting can be deduced from the curves in Fig. 2. For a drain voltage of about +5.5 V, R_{11} = 680Ω to set a drain current of about 1.5 mA at U_{GS} = 1 V. It should be noted, however, that FETs in the same I_{DSS}-U_P group (here, the A-type of the BF256 is used) are subject to a certain production tolerance. Fortunately, this is of little consequence in this case because of the low drive level (below 1 mV).

Measurement amplifier

This consists of a differential amplifier, T_2-T_3, followed by a class-A output amplifier. The emitter current of the differential amplifier is sunk by current source T_4, which uses a LED, D_3, to supply a reference voltage of 1.8 V. A normal red LED has a typical voltage drop of about 1.5 V and can not be used in this application. The LED required is either a high-efficiency or an amber type which drops typically 1.8 V.

With R_{13} = 1 kΩ, T_4 sinks a constant current of 1.2 mA. The output stage also uses a constant current source, T_6. This current source forms a high AC resistance at the collector of T_5. Compared to a single collector resistor, the current source allows a much higher gain to be achieved. The previously mentioned reference voltage source, D_3, is also used for this second current source to give a constant current of about 2.5 mA (1.2 V/R_{19}).

The input FET is DC-coupled to the measurement amplifier and thus determines the bias setting by means of its drain voltage of between 4 V and 5 V. The inverting input of the 'discrete opamp', T_2–T_6, is formed by the base of T_3. This is DC-coupled to the output of the measurement amplifier by feedback resistor R_{15}, so that the differential amplifier regulates the direct voltage at the output (collectors of T_5-T_6) to the value that exists at the non-inverting opamp input, the base of T_2.

The overall gain for alternating voltages is either 83 times or 26 times as determined by switch S_2, which selects feedback resistors R_{15}-R_{16} or R_{15}-R_{17} in series with a parallel combination of capacitors, C_{17}-C_{18}. This simple switch arrangement results in two sets of measurement ranges.

Fortunately, the transistors offer stable operation at relatively high frequencies, so that frequency compensation with a small ceramic capacitor is not needed in the AC feedback network. In practice, C_{14} alone does the job adequately.

Active rectifier

The signal rectifier is capacitively coupled to the measurement amplifier by C_{20} and C_{21}. The active part consists of a two-stage amplifier around T_7-T_8, which uses the rectifier and the moving-coil meter as part of its feedback network to achieve linear operation. The result is a high sensitivity of about 21 mV at the input of the rectifier for full-scale deflection (f.s.d.) of the moving-coil meter. The double meter scale is virtually linear, as shown on the front-panel layout in Fig. 3.

The high as well as stable amplification of the instrument results in a measure-

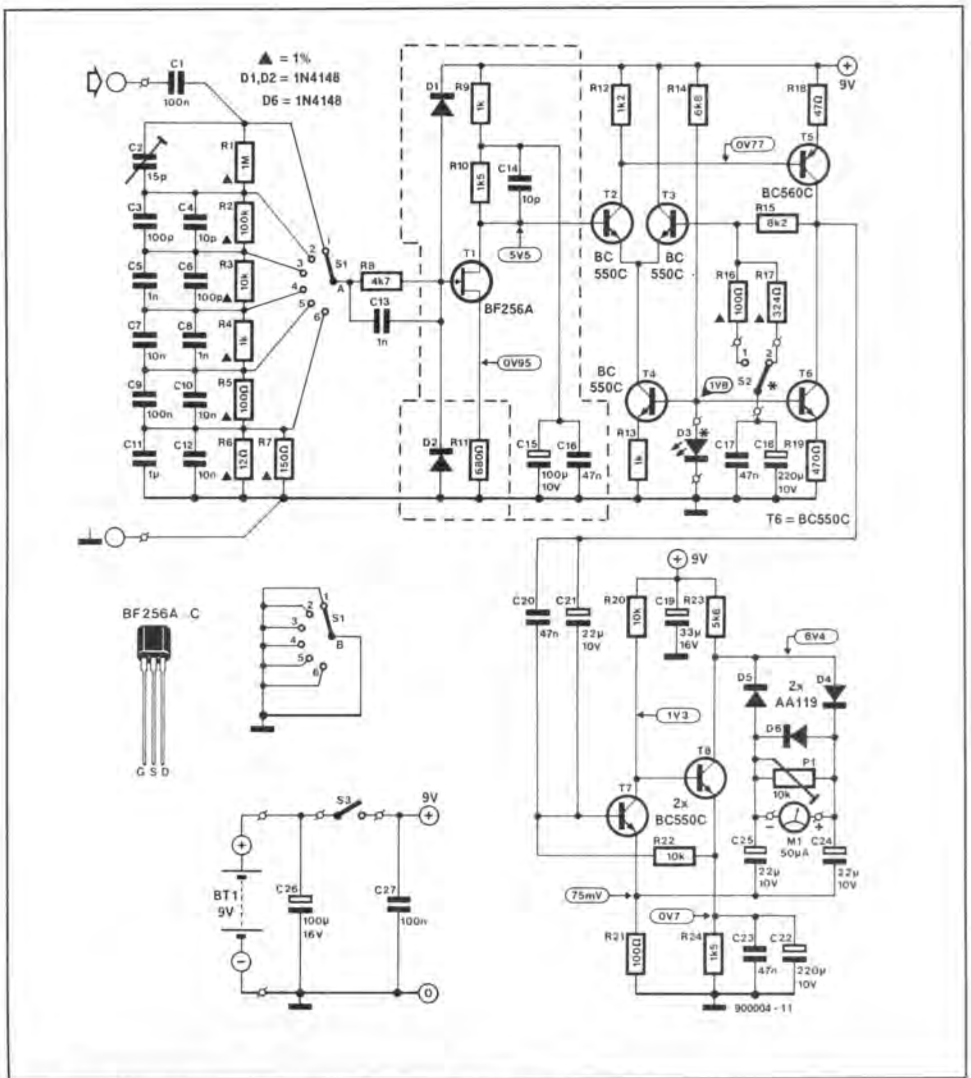


Fig. 1. Circuit diagram of the wideband millivoltmeter.

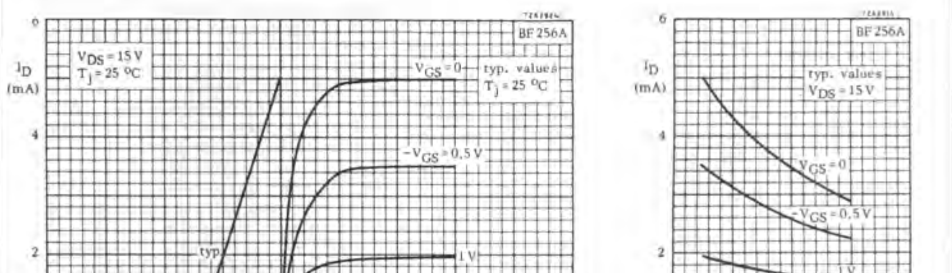


Fig. 2. BF256A FET design data.

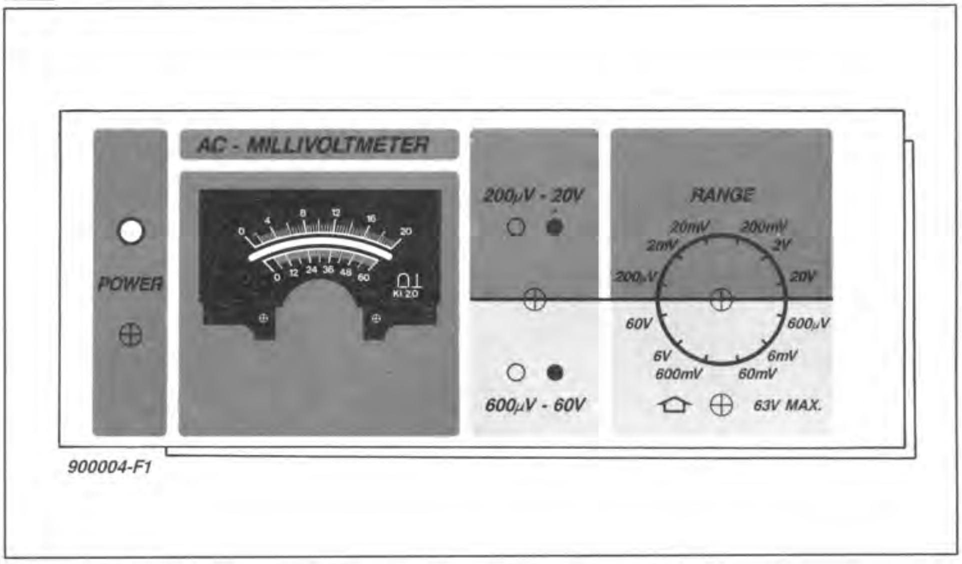


Fig. 3. Front-panel lay-out (shown at approx. 60% of true size).

ment range of 200 µV f.s.d., in which the lowest signal level that can be measured reliably is determined by the noise levels that exist in the discrete opamp and, of course, in the power supply. Consequently, the meter will not normally indicate '0' in the 200 µV range. Capacitors C_{26} and C_{27} reduce the noise on the supply voltage lines and compensate the negative effect of the rising internal resistance of the battery as this is slowly discharged.

Preset P_1 determines the form factor, i.e., it allows the meter indication to be reduced from the peak-to-peak value to the corresponding rms value. Note, however, that the set form factor is only valid for sine-wave voltages: the AC millivoltmeter does not contain a true-rms converter.

The signal rectifier consists of germanium diodes D_4-D_5. Silicon diode D_6 protects the coil in the meter against overloading.

Construction and alignment

As with the previous two instruments in this series, the construction depends entirely on the combination of the printed-circuit board (Fig. 4), the metal enclosure and the front-panel layout (Fig. 3). Together, these give a compact instrument that is simple to build because the wiring is kept to a minimum.

The two rotary switches are 6-way types with a special ring to set the number of positions. Set the ring to two positions on S_2. The same ring may be omitted or set to six positions in the case of the range selector, S_1. Select two suitable collet knobs for the switches and provide them with an additional pointer arrow opposite the one already printed on the plastic collar.

The population of the single-sided printed-circuit board should not present problems. Be sure to fit all components as close as possible to the board, i.e., keep all component terminals as short as possible. Check your work every now and then to prevent a long fault-finding session later.

Fit solder pins at the locations shown between the rotary switches. Next, bend a 20-mm high piece of tin plate to form the screening as shown on the photographs of the prototype board.

Cut and drill a suitable aluminium support plate that can be bolted on to the side panels of the LC-850 enclosure. The completed PCB is fitted on to this support plate with the aid of four 10-mm high threaded PCB spacers.

Use the front-panel foil as a template to cut and drill the aluminium front panel of the enclosure. Fit the power LED, the on/off switch, the moving-coil meter and the BNC socket. Connect wires to the LED, the switch and the meter, and a short length of screened cable to the BNC socket.

Remove the rear panel of the enclosure, and insert the support plate with the PCB on it vertically between the side brackets of the enclosure. Move the assembly towards the front of the enclosure until the PCB is at about 50 mm from the front panel. This position allows enough room for the body of the moving-coil meter. Mark the holes in the side brackets to be used for securing the support panel. Cut the rotary switch spindles at the required distance from the front panel. Check if the two collet knobs fit, and remove them again.

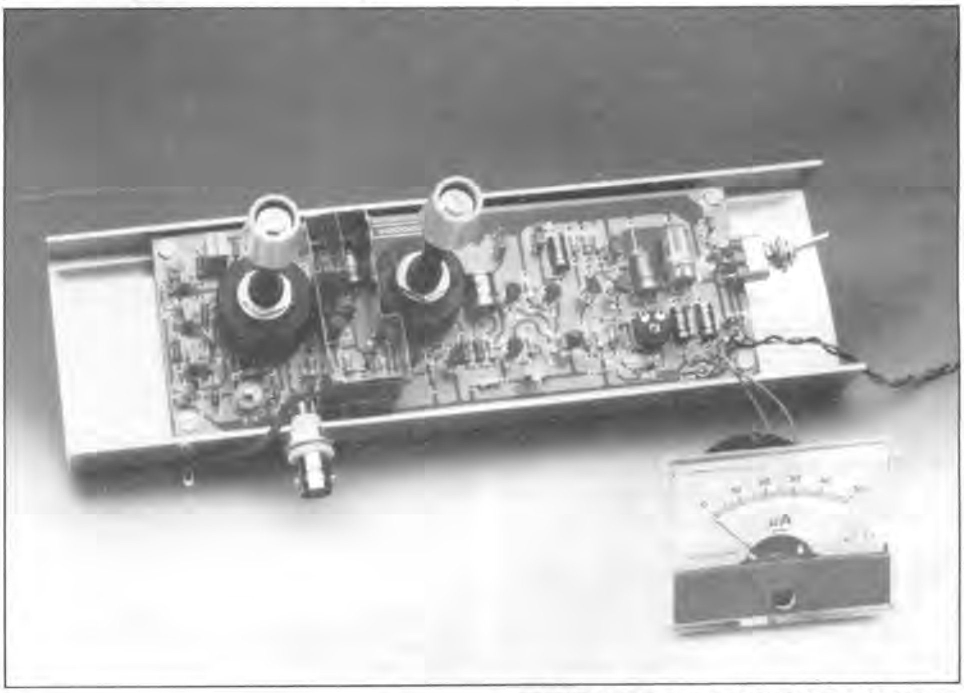
The enclosure has ample room behind the vertically fitted support plate for a 9-V battery or a battery pack made up of six penlight types. Rechargeable batteries may also be used, in which case it is necessary to fit a charge socket on the rear panel of the enclosure. The AC millivoltmeter must never be powered by a mains adapter without an internal 9 V regulator.

Setting up

The instrument is aligned before it is re-assembled and fitted into the enclosure. Connect the meter, the on/off switch, the LED, the BNC socket and a 9-V battery. Fit the knobs provisionally on the switch spindles.

Switch on, and check that the current consumption is 7–8 mA. Use a digital multimeter to measure the voltage at the anode of D_3 (+1.8 V) and the positive terminal of C_{21} (between +5 V and +6 V). The latter voltage must be virtually equal to that at the drain of T_1. If this is not the case, replace the FET, or adapt R_{11}. Check that the collector of T_8 is at about +6.4 V.

Set the instrument to the 60 V range and adjust the mechanical meter setting to an indication of 0. Connect a sine-wave generator to a digital multimeter set to alternating voltage measurement. Set the generator to a frequency between 100 Hz and 200 Hz. Connect a 1000:1 voltage divider between the input of the DMM and the input of the AC millivoltmeter. This voltage divider consists of a 10 kΩ- and a 10 Ω resistor (both at 1% tolerance). Set the millivoltmeter to the 0.6 V range and the DMM to the 1 V or 3 V range. Adjust preset P_1 for corresponding readings on the DMM and the AC millivolt-



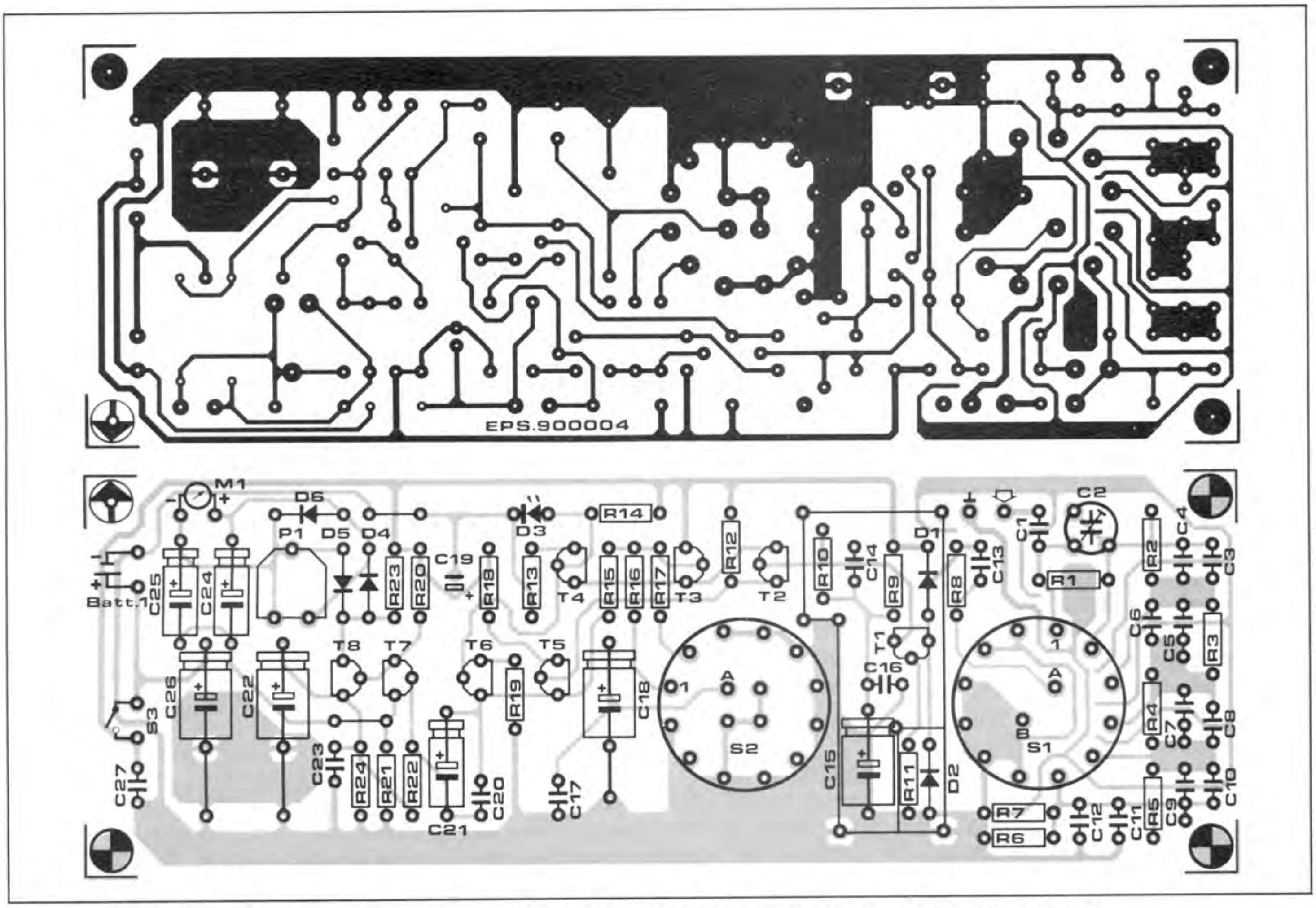


Fig. 4. Track layout and component mounting plan of the single-sided printed-circuit board for the millivoltmeter.

meter — i.e., disregard the multipliers 1 (V) and 0.001 (mV) — and check the adjustment for a couple of amplitude settings on the generator.

Check the indications on the millivoltmeter against those on the DMM. If the meter scale deviates considerably, try fitting another pair of diodes in positions D_4 and D_5 (Types BAT85 may be used if the stated germanium diodes are hard to obtain).

Since 1%-tolerance resistors are used in the input attenuator, the indications in the other ranges follow the results of the above alignment to within 1%.

Trimmer C_2 is adjusted for optimum compensation at an input frequency of 200 kHz. An oscilloscope and a sine-wave oscillator are required for this calibration to compare the indicated levels in the 200 mV ranges. If these instruments are not available, set C_2 to about two-thirds of its range to give a capacitance of 10–12 pF.

The prototype shown in the photographs has a 1-dB bandwidth of over 4 MHz, and an indication error smaller than 5% at 2 MHz.

Previously featured test equipment in this series:

RF inductance meter. *Elektor Electronics* October 1989.

LF/HF signal tracer. *Elektor Electronics* December 1989.

Parts list

Resistors:

R_1 = 1M0; 1%
R_2 = 100k; 1%
R_3 = 10k; 1%
R_4 = 1k0; 1%
R_5;R_{16} = 100Ω; 1%
R_6 = 12Ω; 1%
R_7 = 150Ω; 1%
R_8 = 4k7
R_9;R_{13} = 1k0
R_{10};R_{24} = 1k5
R_{11} = 680Ω
R_{12} = 1k2
R_{14} = 6k8
R_{15} = 8k2
R_{17} = 342Ω; 1%
R_{18} = 47Ω
R_{19} = 470Ω
R_{20};R_{22} = 10k
R_{21} = 100Ω
R_{23} = 5k6
P_1 = 10k preset H

Capacitors:

C_1;C_{27} = 100n ceramic
C_2 = 15p trimmer
C_3 = 100p polystyrene (styroflex)
C_4;C_{14} = 10p
C_5 = 1n0
C_7 = 10n
C_6 = 100p
C_8;C_{13} = 1n0 ceramic
C_9 = 100n
C_{10};C_{12} = 10n ceramic
C_{11} = 1µ0
C_{15} = 100µ; 10 V
C_{16};C_{17};C_{20};C_{23} = 47n ceramic
C_{18};C_{22} = 220µ; 10 V
C_{19} = 33µ; 16 V tantalum bead
C_{21};C_{24};C_{25} = 22µ; 10 V
C_{26} = 100µ; 16 V

Semiconductors:

D_1;D_2;D_6 = 1N4148
D_3 = amber or high-intensity LED
(U_f = 1.8 V; see text)
D_4;D_5 = AA119
T_1 = BF256A
T_2;T_3;T_4;T_6;T_7;T_8 = BC550C
T_5 = BC560C

Miscellaneous:

S_1;S_2 = 2-pole 6-way rotary switch for PCB mounting.
S_3 = miniature SPDT switch.
BT_1 = 9-V battery with clip.
M_1 = 50 µA moving-coil meter e.g., Monacor Type PM2.
Metal enclosure: H=80 mm; W=200 mm; D=180 mm. E.g., Telet LC-850 (C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland).
PCB Type 900004 (see Readers Services page).
Front-panel foil 900004-F (see Readers Services page).

ALL-SOLID-STATE PREAMPLIFIER

PART 2 – VOLUME CONTROL STAGES

by T. Giffard

In this second and final part of the article we describe the volume and balance control stages, followed by the construction of the complete preamplifier.

Like the CMOS switches described in Part 1, the volume control switches are connected in an amplifier circuit in such a way that they have no potential drop across them. This results in very low distortion, so that the preamplifier can be used in top-quality stereo installations.

The basic principle of the volume control circuit is illustrated in Fig. 9. Since it is not easy to design an electronic switch with, say, fifty positions, two cascaded attenuation networks, each consisting of eight voltage dividers, are used.

Each network is switched in steps of 1.25 dB and the second (coarse) in steps of 10 dB. When the 'fine' attenuator reaches maximum attenuation (8 × 1.25 =10 dB), the 'coarse' one is switched by one step (= 10 dB). A total attenuation of 78.75 dB in 8 × 8 = 64 steps is therefore provided. This number of steps could not be provided by a standard rotary switch.

Each attenuator section is resistively coupled to the input of an 8-to-1 multiplexer. The output of each multiplexer is applied to the inverting input of an op-amp, so that there is no voltage drop across the multiplexers.

A control circuit ensures that the multiplexers are switched correctly and that the attenuators for the left- and right-hand channels can be used independently with the aid of balance switches.

A preset key makes it possible for the volume to be set to a predetermined position.

Circuit description

In the circuit diagram of Fig. 10, the buffered signals from the input circuits are fed to the 'fine' attenuator (R94 –R101 for

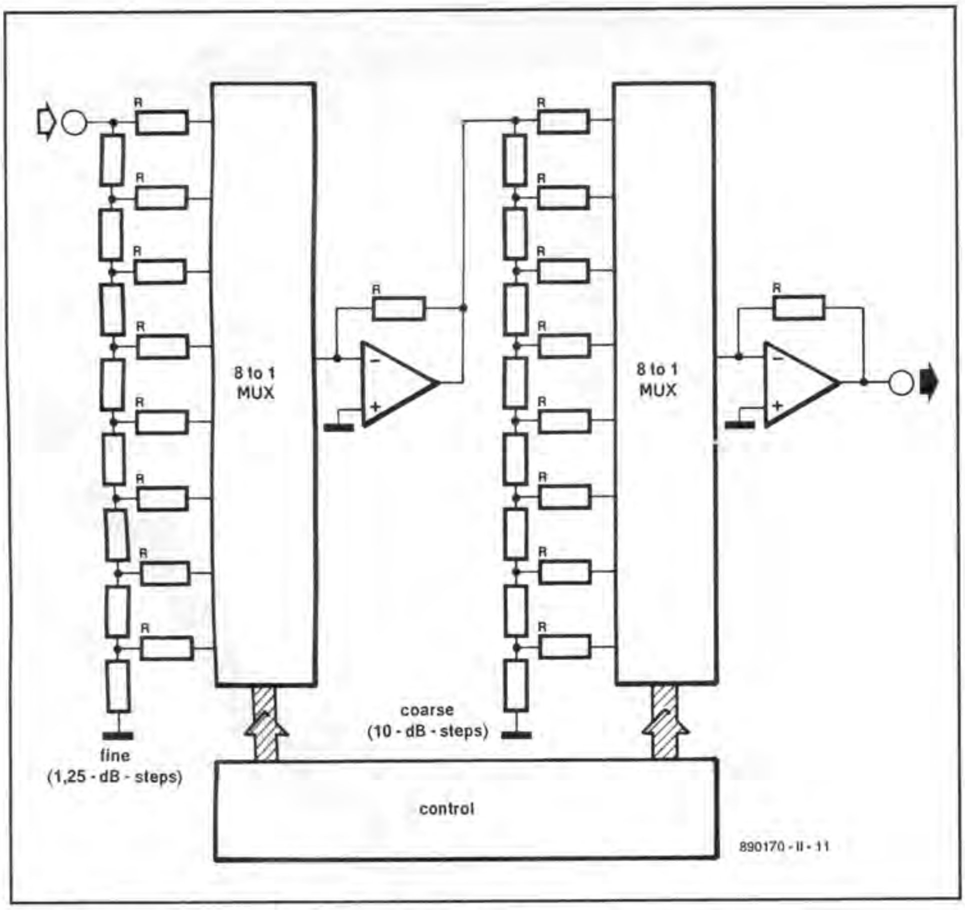
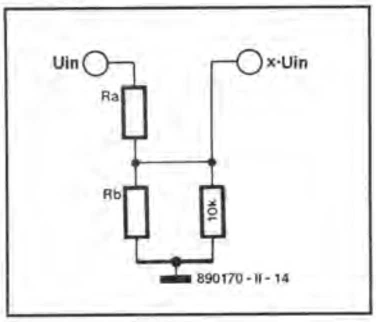


Fig. 9. Fundamental set-up of the volume control circuit.

Calculation of voltage dividers

Each of the voltage dividers in the attenuators of Fig. 9 is basically configured as shown below.



Each voltage divider is formed by resistors R_a and R_b, the ratio of whose values depends on which branch of the divider they are located in. The 10 kΩ resistor is connected via the multiplexer to the inverting input of the opamp (virtual earth), so that, as far as the potential divider is concerned, it is connected to earth.

The voltage at the junction of the resistors is xU_{in}, where x is the attenuation factor (no attenuation: $x = 1$; maximum attenuation: $x = 0$).

In the computation, the value of $R_a + R_b$ is taken as 10 kΩ, which gives a value for x of:

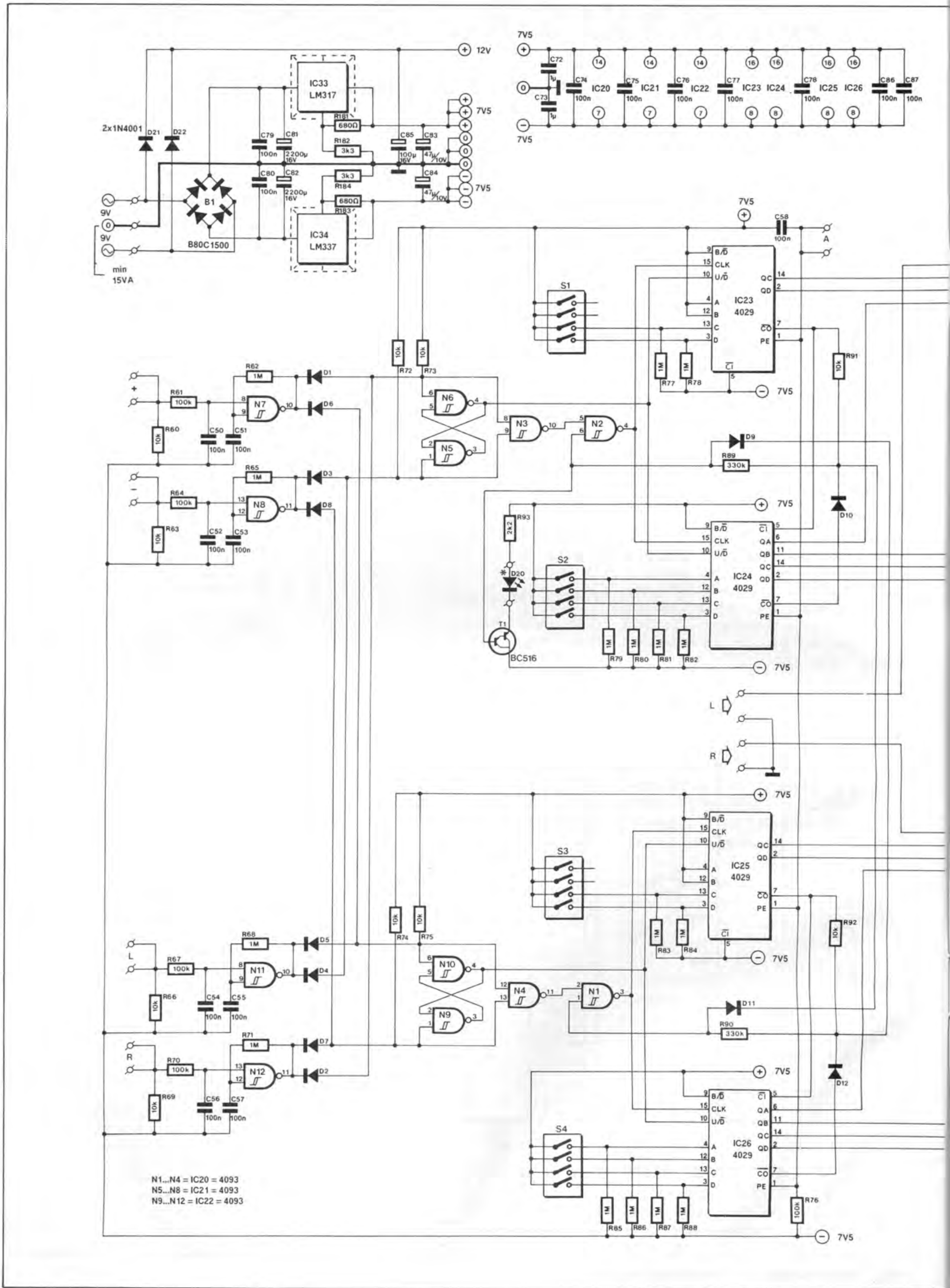
$$x = \frac{R_b // 10\,\text{k}\Omega}{R_b // 10\,\text{k}\Omega + R_a}$$

and for R_a of $(10\,\text{k}\Omega - R_b)$.

Substituting these values and rearranging the formula for x, gives a value (in kΩ) for R_b of:

$$R_b = \frac{10 - \frac{10}{x} + \sqrt{\left(\frac{10}{x} - 10\right)^2 + 400}}{2}$$

If it is desired to change the value of the steps, x must be replaced by $10^{y/20}$, where y is the desired attenuation in dB per step. Remember that from the result for each step the result of the previous step must be deducted. Resistance values so calculated must, where necessary, be rounded to the nearest standard value.


12V
7V5
0
2x1N4001
D21
D22
B1
B80C1500
9V
9V
min
15VA
IC33
LM317
IC34
LM337
R181
680Ω
R182
3k3
R184
3k3
R183
680Ω
C79
100n
C81
2200µ
16V
C80
100n
C82
2200µ
16V
C85
100µ
16V
C83
47µ
10V
C84
47µ
10V
C72
1µ
C73
1µ
C74
100n
C75
100n
C76
100n
C77
100n
C78
100n
C86
100n
C87
100n
IC20
IC21
IC22
IC23
IC24
IC25
IC26
14
16
7
8
C58
100n
A
S1
S2
S3
S4
IC23
4029
IC24
4029
IC25
4029
IC26
4029
B/D̄
CLK
U/D̄
QA
QB
QC
QD
C̄O
C̄I
PE
R77
1M
R78
1M
R79
R80
R81
R82
R83
R84
R85
R86
R87
R88
R91
10k
R92
10k
R76
100k
D9
D10
D11
D12
R89
330k
R90
330k
R93
2k2
D20
T1
BC516
L
R
+
−
R60
10k
R61
100k
R62
1M
R63
10k
R64
100k
R65
1M
R66
10k
R67
100k
R68
1M
R69
10k
R70
100k
R71
1M
R72
10k
R73
10k
R74
10k
R75
10k
C50
C51
C52
C53
C54
C55
C56
C57
100n
D1
D2
D3
D4
D5
D6
D7
D8
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
N12
N1...N4 = IC20 = 4093
N5...N8 = IC21 = 4093
N9...N12 = IC22 = 4093

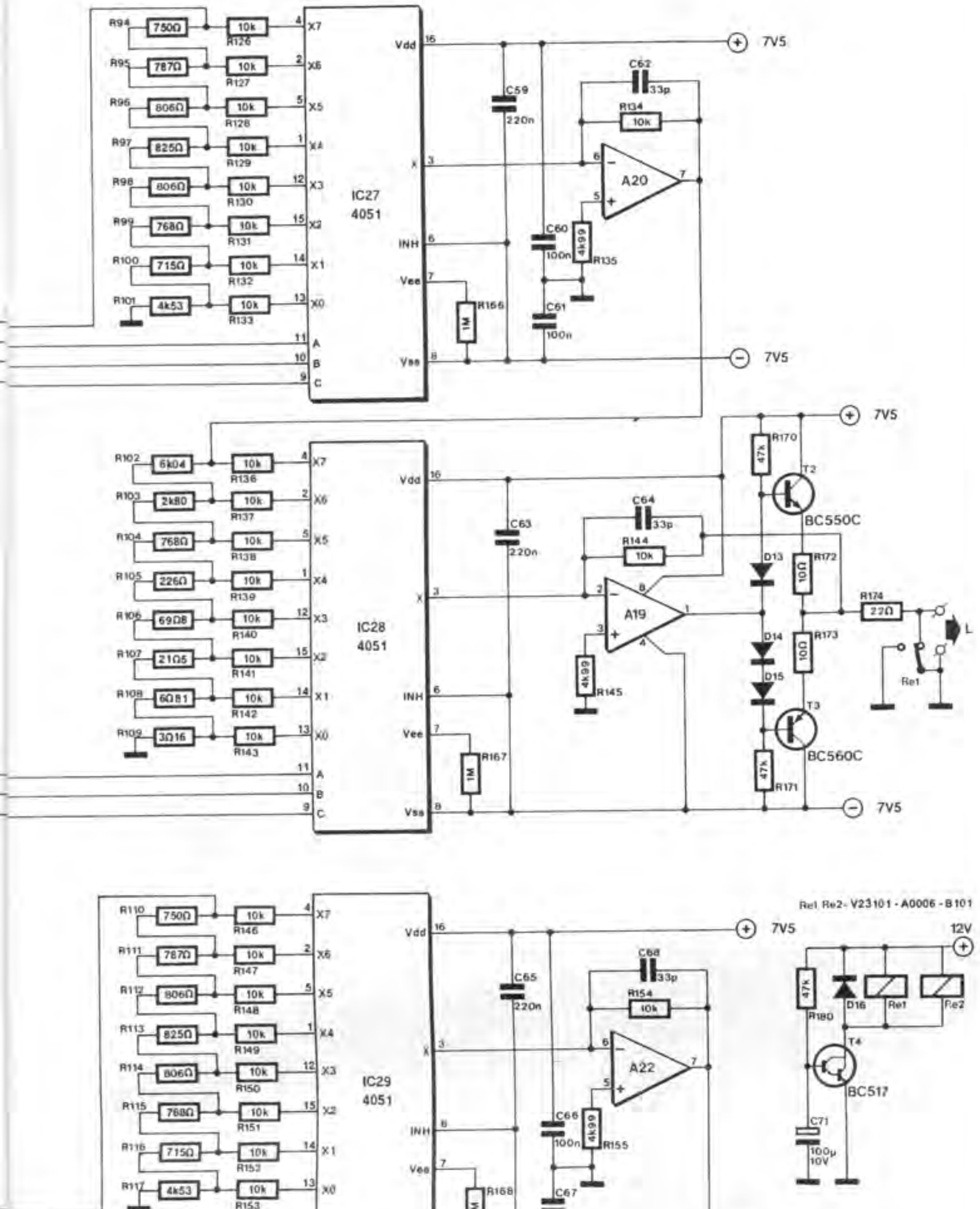


Fig. 10. Circuit diagram of the volume and balance control stages.

the left-hand channel and R110–R117 for the right-hand channel). Each branch of the attenuator is connected via a 10 kΩ resistor to the first multiplexer (IC27 and IC29 for the left-hand and right-hand channels respectively. The output of the 'fine' attenuators is applied to the 'coarse' attenuators, R102–R109 and R118–R125, via buffers A20 and A22 respectively. The output of the 'coarse' attenuators is applied to a second multiplexer, IC28 and IC30 respectively, each of which is followed by a buffer, A19 and A21.

Buffers A19 and A21 are configured rather differently from A20 and A22, in that they have an additional, complementary pair of transistors, T2-T3 and T5-T6.

The three diodes between the bases of these transistors ensure an adequate quiescent current.

The output impedance of these circuits is very low, so that long leads to the power amplifiers will not cause any problems.

The 22 Ω resistors, R174 and R179, provide short-circuit protection. The outputs may be connected direct to 600 Ω headphones.

The relay contacts at the outputs connect the outputs to earth to obviate audible clicks when the mains is switched on or off. It was not possible to replace the relay by an electronic device. Fortunately, the contacts are not in the signal path, so that the sound quality can never be affected by them.

The multiplexers are switched by Type 4029 preset up/down counters: IC23-IC24 for the left-hand channel and IC25-IC26 for the right-hand channel. DIP switches allow the volume to be preset to individual taste. Each time the preamplifier is switched on or when the reset key is pressed, the preset counter positions are assumed.

The carry-out pins of the counters are interconnected in a manner to ensure that the gates which provide the clock pulses, N2 for IC23-IC24 and N1 for IC25-IC26, are both blocked the moment one of the counters reaches nought or maximum. This arrangement ensures that the balance setting is maintained when the volume is adjusted to nought or maximum.

The plus and minus volume keys are connected to start/stop oscillators N7 and N8 respectively. A momentary depression of a key causes a single pulse at the output of the associated gate, while a sustained depression causes a pulse train. If the speed of this control is found to be too low, it may be increased by lowering the value of C51 and C53, and possibly also of C55 and C57.

The pulses associated with the +key are fed to N3 via D1 and to N4 via D6. The ensuing signals are taken to the clock inputs of the counters via

N_2 and N_1 respectively.

When the –key is pressed, the generated pulses are passed to the clock inputs of the counters via D_3-N_3-N_2 and D_8-N_4-N_1 respectively.

Two bistables, N_5-N_6 for the left-hand channel and N_9-N_{10} for the right-hand channel, provide a signal that drives the up/down inputs of the counters. The level of this signal depends on which key is pressed.

The circuit of the balance control is virtually identical with that of the volume control. An exception is that the bistables are configured in a way that causes the left-hand counter to receive an 'up' signal when the right-hand counter gets a 'down' signal. Thus, if the left-hand balance key is pressed, the left-hand counter counts up and the right-hand counter counts down. Pressing the reset key returns the circuits to the position set by S_1–S_4. That position need not be the same for the two channels. This is useful where, for instance, there is a small difference in balance between the two speakers.

The power supply provides a separate voltage for energizing the output relay. Because of the (relatively) low value of C_{85}, the relay is deenergized immediately the mains is switched off. On power-up, there is a delay provided by R_{180}-C_{71}-T_4.

The remainder of the preamplifier is powered by the regulated, symmetrical voltage provided by IC_{33} and IC_{34}.

Construction

Populating the PCB shown in Fig. 11 should not present any problems. All ICs and DIL switches may be mounted in sockets, but this is not obligatory.

The two electrolytic capacitors in the power supply are types that should be mounted upright. Each of the regulator ICs should be fitted on a heat sink.

It is convenient to provide all connexion points with a solder pin. Not, by the way, that for each control signal two solder pins may be fitted: this will facilitate the possible extension with remote control at a later date.

It is advisable to set all DIP switches to zero before the board is installed in the enclosure. The counters are then at nought at first power-up and that is a safe starting point.

The preamplifier may be installed in a 19-inch, 2-unit (88 mm) high, enclosure. The enclosure used for the prototypes – see Fig. 12 – has a double front panel. Rectangular holes are cut in the back of this panel over which the control boards are screwed. If an enclosure with a single front panel is used, the three control boards may be fitted direct to the rear of the panel with the aid of small metal brackets.

The LED located on the board with the volume and balance controls should be bent sideways by a few millimetres so that it comes directly behind the relevant opening in the front panel.

Note that self-adhesive foils for the front and rear panels of the enclosure are available through the Readers' service (see Fig. 13).

The boards for the input and system control stages dealt with in Part 1 should be fitted near the left-hand side of the rear panel.

The board for the volume and balance control stages should be fitted at the left-hand centre of the enclosure in such a way that the relays are located nearest the input boards. The mains transformer, the mains on-off switch and the mains cable entry should be fitted at the extreme right-hand rear of the enclosure, as far away as possible from the printed-circuit boards.

Note that the mains earth should be connected only to the appropriate terminal on the volume control board.

A wiring diagram for the complete preamplifier is shown in Fig. 14. For all analogue signals suitable screened cable should be used; all other connexions may be made in standard insulated circuit wire.

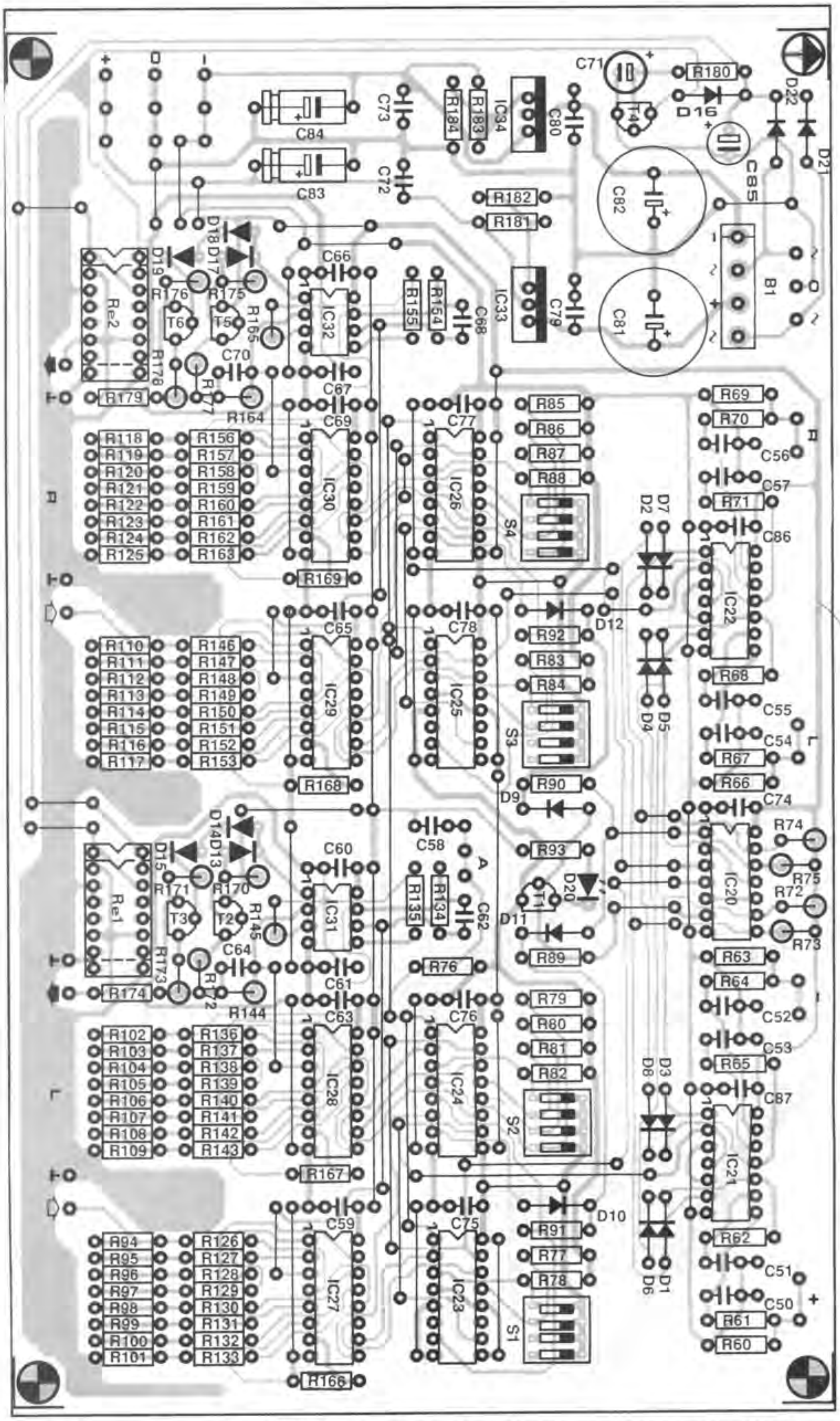


Fig. 11. Component mounting side of the printed-circuit board for the volume and balance control.

Parts list

Resistors:
R_{60};R_{63};R_{66};R_{69};R_{72} – R_{75};R_{91};R_{92} = 10k
R_{61};R_{64};R_{67};R_{70};R_{76} = 100k
R_{62};R_{65};R_{68};R_{71};R_{77} – R_{88};
 R_{166} – R_{169} = 1M0
R_{89};R_{90} = 330k
R_{93} = 2k2
R_{94};R_{110} = 750Ω; 1%
R_{95};R_{111} = 787Ω; 1%
R_{96};R_{98};R_{112};R_{114} = 806Ω; 1%
R_{97};R_{113} = 825Ω; 1%
R_{99};R_{104};R_{115};R_{120} = 768Ω; 1%
R_{100};R_{116} = 715Ω; 1%
R_{101};R_{117} = 4k53; 1%
R_{102};R_{118} = 6k04; 1%
R_{103};R_{119} = 2k80; 1%
R_{105};R_{121} = 226Ω; 1%
R_{106};R_{122} = 69Ω8; 1%
R_{107};R_{123} = 21Ω5; 1%
R_{108};R_{124} = 6Ω81; 1%
R_{109};R_{125} = 3Ω16; 1%
R_{126} – R_{134};R_{146} – R_{154};
 R_{156} – R_{164} = 10k; 1%
R_{135};R_{145};R_{155};R_{165} = 4k99; 1%
R_{170};R_{171};R_{175};R_{176};R_{180} = 47k
R_{172};R_{173};R_{177};R_{178} = 10Ω; 0.6 W
R_{174};R_{179} = 22Ω; 0.6 W
R_{181};R_{183} = 680Ω
R_{182};R_{184} = 3k3

Capacitors:
C_{50} – C_{58};C_{60};C_{61};C_{66};C_{67};C_{74} – C_{80};
 C_{86};C_{87} = 100n
C_{59};C_{63};C_{65};C_{69} = 220n
C_{62};C_{64};C_{68};C_{70} = 33p
C_{71} = 100μ; 16 V; radial
C_{72};C_{73} = 1μ0; MKT
C_{81};C_{82} = 2200μ; 16 V; radial
C_{83};C_{84} = 47μ; 10 V
C_{85} = 100μ; 16 V; radial

Semiconductors:
D_{1} – D_{19} = 1N4148
D_{20} = LED; red; 3 mm
D_{21};D_{22} = 1N4001
B_{1} = B80C1500
T_{1} = BC516
T_{2};T_{5} = BC550C
T_{3};T_{6} = BC560C
T_{4} = BC517
IC_{20} – IC_{22} = 4093
IC_{23} – IC_{26} = 4029
IC_{27} – IC_{30} = 4051
IC_{31};IC_{32} = NE5532
IC_{33} = LM317
IC_{34} = LM337

Miscellaneous:
S_{1} – S_{4} = 4-way DIP switch block.
Re_{1};Re_{2} = PCB-mount 12-V relay: e.g. Siemens V23101-A0006-B101.
Qty 2: heatsink (for IC_{33} and IC_{34}).
Tr1 = toroidal transformer 2×9 V @15 VA: e.g. Type 03011 (240 V mains; Jaytee Electronic Services) or Type 01011 (220 V mains).
Enclosure: 25 or 30 cm deep: e.g. ESM Type ER48/09.
Fused chassis plug for mains cord: e.g. ElectroMail stock no. 481-639.
Fuse: 100 mA slow.
PCB Type 890170-2 (see Readers Services page).
Front and rear panel foils Types 890170-F1 and -F2 (see Readers Services page).

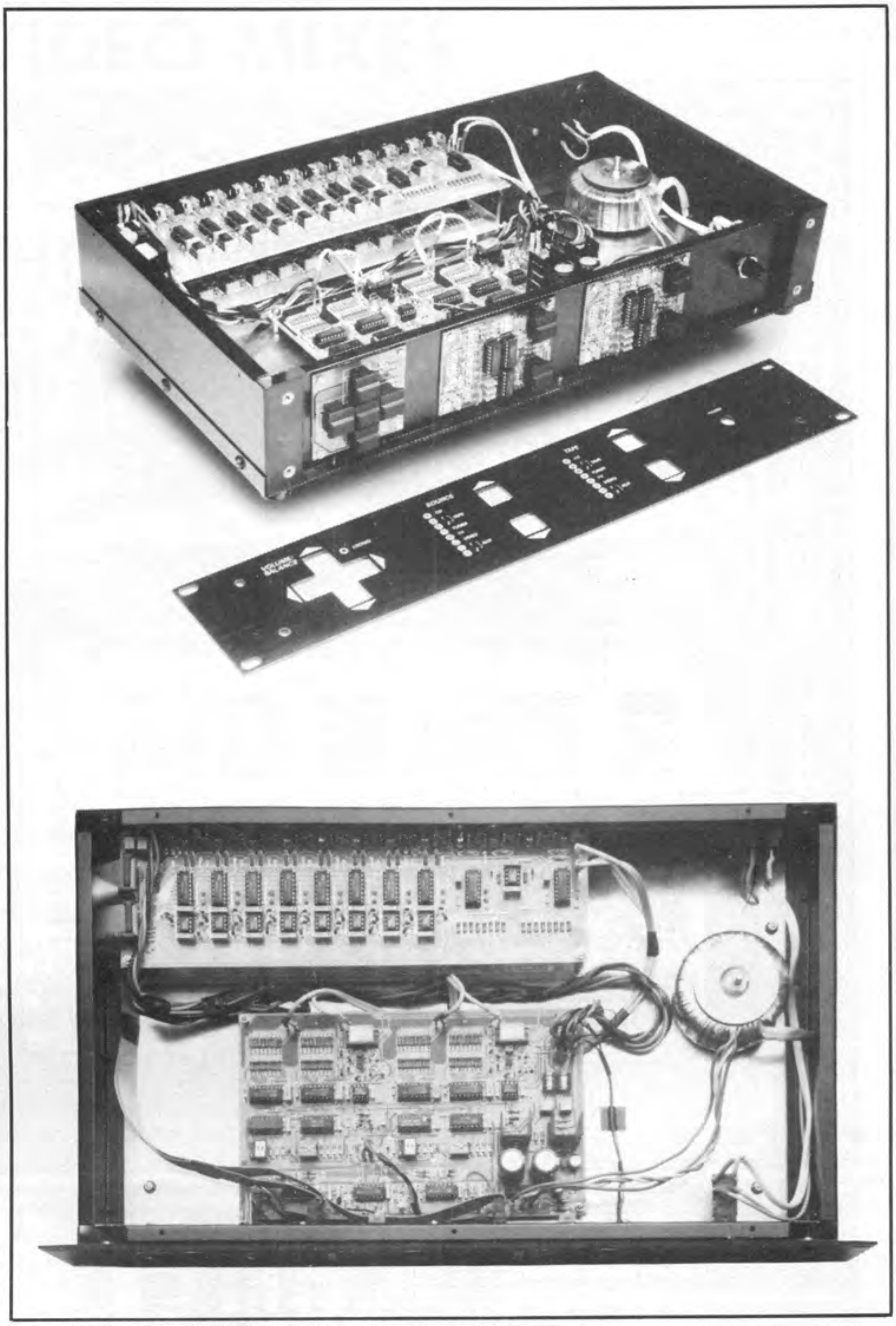


Fig. 12. General views of the prototype of the preamplifier

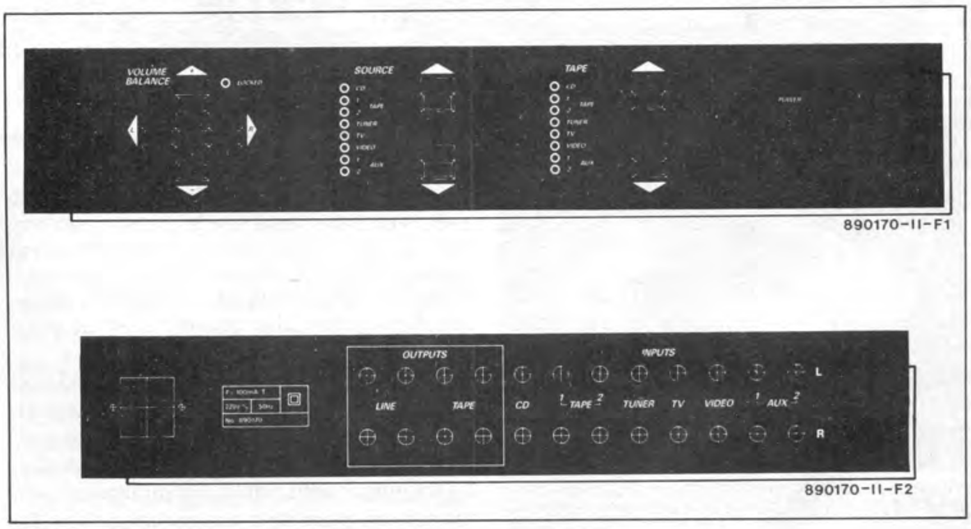


Fig. 13. Self-adhesive foils are available for the front and rear panels.

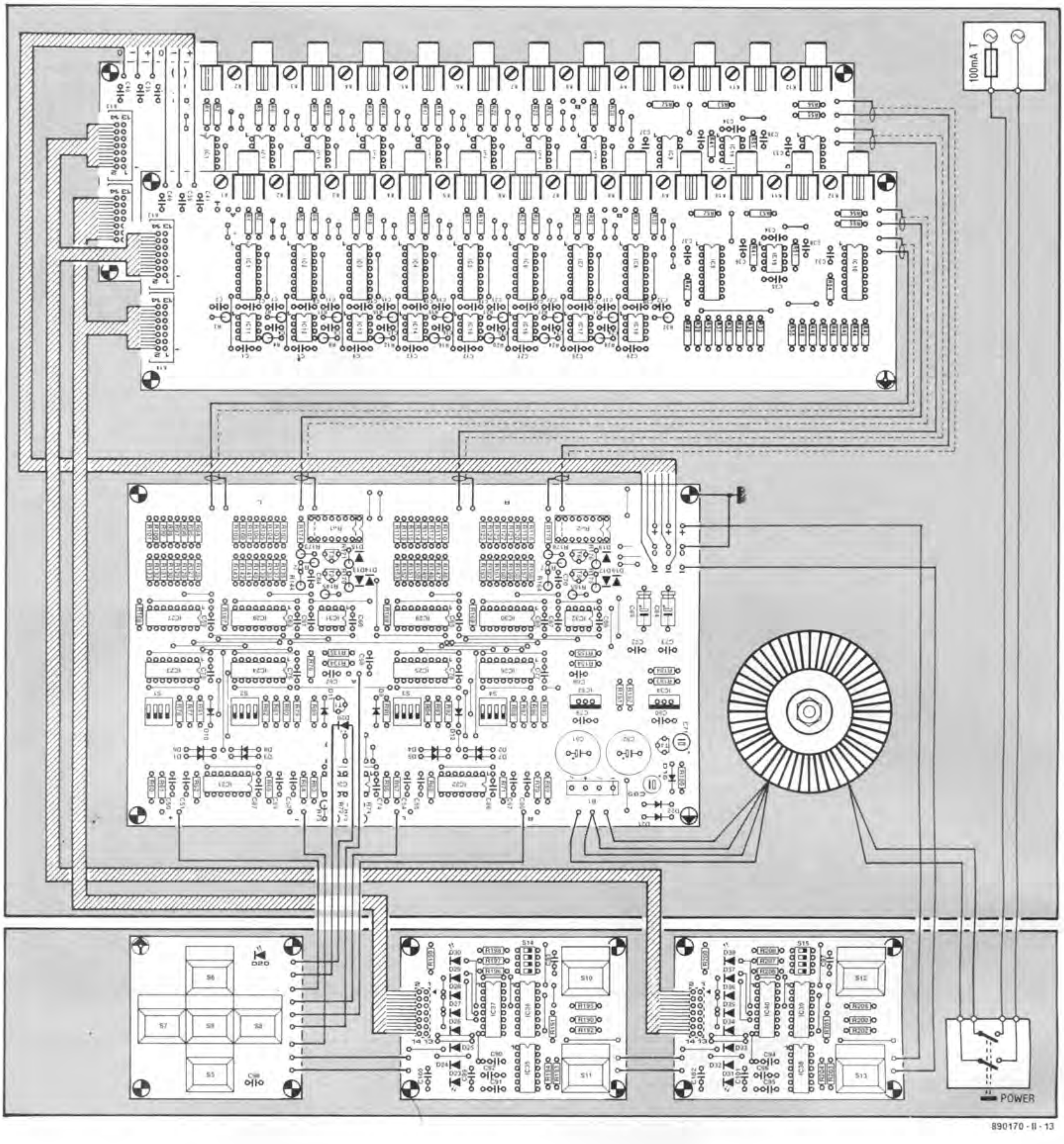


Fig. 14. Wiring diagram for the complete preamplifier.

Some ribbon cables were already described in Part 1 and these may now be shortened where necessary. If the connectors are dismantled carefully, they may be refitted to the (shortened) cable without any problems.

After all the boards are fitted and interconnected, a few simple checks can be carried out. Make sure that DIP switches S2 and S4 are OFF, otherwise there is the likelihood of a deafening sound from the loudspeakers when the preamplifier is connected into the audio system.

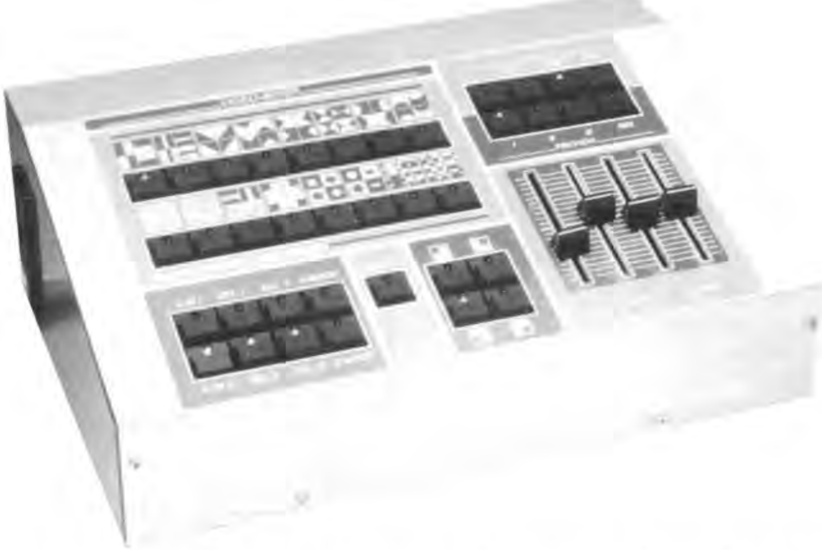
After the mains has been switched on, it should be possible to select all the inputs for tape-out and line-out. The volume and balance controls may also be tested: the LED should light when the minimum and maximum positions are reached. Briefly pressing the reset key should bring the volume back to the preset value.

Finally, you will have noticed that the preamplifier is DC-coupled throughout and normally this should not create any problems. However, if the input of your power amplifier has no capacitors, it may be advisable to connect a couple of good-quality capacitors (for instance, 4.7–10 µF metallized polypropylene or polystyrene types) in the line outputs.

VIDEO MIXER

PART 1: VIDEO SWITCHING BOARD

A. Rigby



Recent developments in consumer electronics have boosted the popularity of video recorders, portable cameras and camcorders to such an extent that the film camera has become a thing of the past. Video enthusiasts who want to edit and mix recorded material from various video sources, and in addition require special fade-in and fade-out effects, will delight in building and using the advanced mixing desk presented here.

Not so long ago, a small fortune would buy a bulky video recorder offering mono sound, a primitive programming facility and just acceptable picture quality if the tracking control was re-adjusted from time to time. Today's camcorders (camera-recorders) cost less than these old VCRs, but offer significantly improved sound and picture quality. Stereo sound, Super-VHS and all-digital recording techniques are already available but will take some time to become established in the consumer markets.

In spite of all its technological benefits, the camcorder has one disadvantage when compared to, say, an 8-mm film camera: editing recordings requires a mixer, of which there appear to be few around that can be purchased ready-made at a reasonable price.

The video mixer/effects unit described here allows a up to three video signals to be combined into one video output signal. The mixer also offers a number of special effects which result in attractive fade-in, fade-out and superimpose effects.

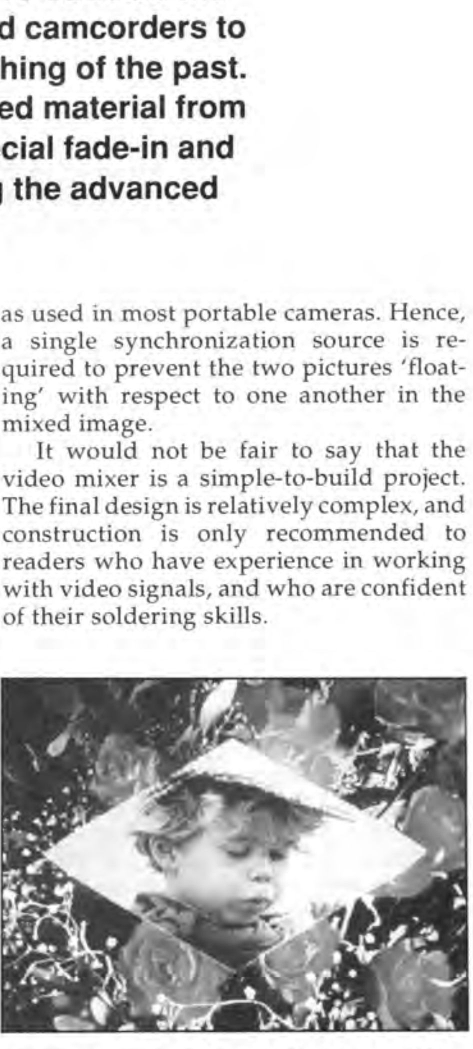
An important proviso must be mentioned at the outset: depending on the number of video sources connected to the mixer, at least one (two sources) or two (three sources) must have an external synchronization input. One video source always serves as the master sync source, the other (one or two) are externally synchronized.

The mixer always mixes two signals, even when three signals are applied. It does not allow three signals to be shown simultaneously. The mixing options are:

- video 1 with video 2
- video 1 with video 3
- video 2 with video 3

Again remember that video sources that lack an external synchronization input can not be mixed. The reason for this is probably familiar to those who have experience working with video signals, but may be less obvious to many other readers. Mixing video signals is essentially alternate switching between lines of two TV pictures. To maintain phase synchronism between the two pictures, their picture line content must start at the same instant. The synchronization pulses in the video signal serve to time this instant. The sync pulse frequencies of the two video sources will not be equal if the syncs are derived from free-running clock circuits as used in most portable cameras. Hence, a single synchronization source is required to prevent the two pictures 'floating' with respect to one another in the mixed image.

It would not be fair to say that the video mixer is a simple-to-build project. The final design is relatively complex, and construction is only recommended to readers who have experience in working with video signals, and who are confident of their soldering skills.



Lozenge-insertion: one of the many picture mixing effects.

Two block diagrams

The basic operation of the video mixer is best understood by looking at the block diagram in Fig. 1. The three blocks shown in the drawing represent the three circuits that make up the video mixer. Each circuit is constructed on a separate printed-circuit board. This first instalment of a four-part article deals with the video switching board. Part 2 discusses the modulation board, and Part 3 the keyboard. Part 4, finally, addresses matters related to the adjustment and practical use of the video mixer.

The block diagram shows four inputs, VIDEO I, VIDEO II, VIDEO III and VIDEO EXP. The first three accept the video signals that are to be mixed. Input VIDEO I takes the master signal that ensures the central synchronization. The video source connected to this input does not require an external synchronization input, and must always be present to provide the master sync signals for the other video source(s). The other two inputs, VIDEO II and VIDEO III, are identical, and take signals from sources synchronized with VIDEO I.

The fourth mixer input, VIDEO EXP (expansion input), takes an additional signal that may be routed to the monitor when none of the other inputs is being used. This 'stand-by' signal may be supplied by a test chart generator or logomat. It can not be mixed with the other channels.

The video mixer has four outputs. The BLACK-BURST (BB-video) output supplies the composite synchronization signal for the video sources. Outputs PROGRAM and MONITOR are electrically identical and supply the mixed video output signal. The PREVIEW output, finally, allows the video-1, video-2, video-3, or the mixed video signal to be viewed independently of the other outputs.

The video switching board divides the synchronization signal recovered from video-1 between the sub-circuits. The control signals for the modulation and the switching board emanate from the keyboard circuit (to be discussed in Part 3). The function of these control signals, marked SCxx, will be reverted to in due course.

Figure 2 shows the block diagram of the video switching board. The input buffers are at the left, the outputs at the right. Electronic switches at a number of locations select the required signals. The control blocks at the top of the diagram are used to generate the sync signals and enable the colour burst in the master signal to be inserted at the right instant into the output signal. In the mixer circuit, the horizontal and vertical sync signals are available separately in true as well as inverted form. The KEYOUT output allows a kind of picture-in-picture effect to be achieved: one particular colour is removed from the picture on one channel, to be filled in by corresponding areas in the picture on the other channel. This effect is often used in TV news broadcasts to create a background for (apparently large)

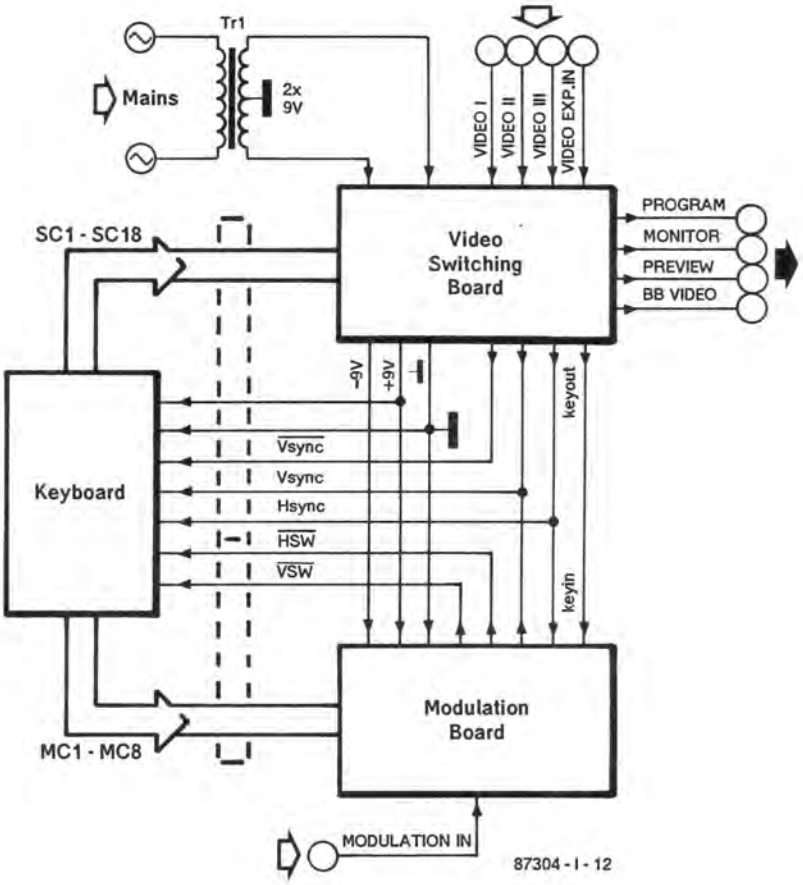


Fig. 1. Block diagram of the video mixer. The circuit is accomodated on three printed-circuit boards.

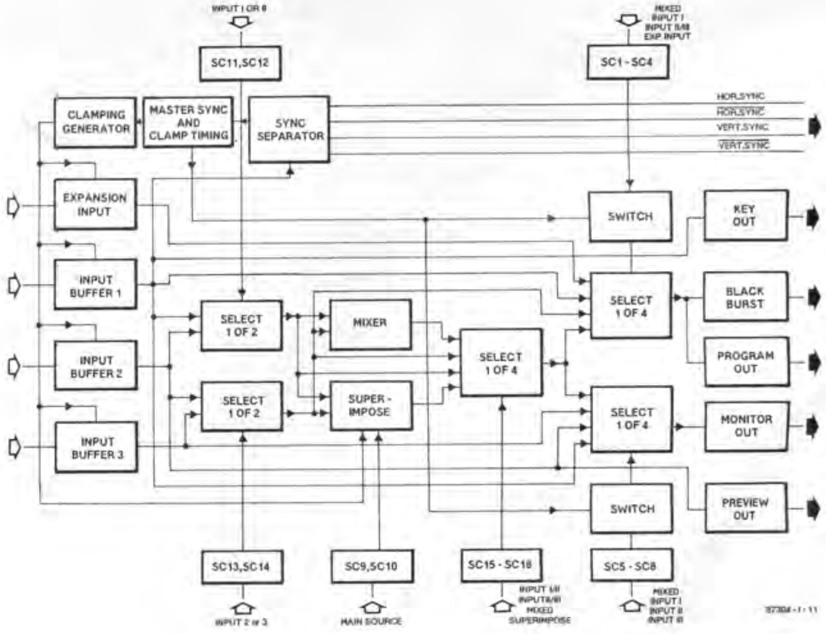


Fig. 2 Block diagram of the first module, the video switching board.

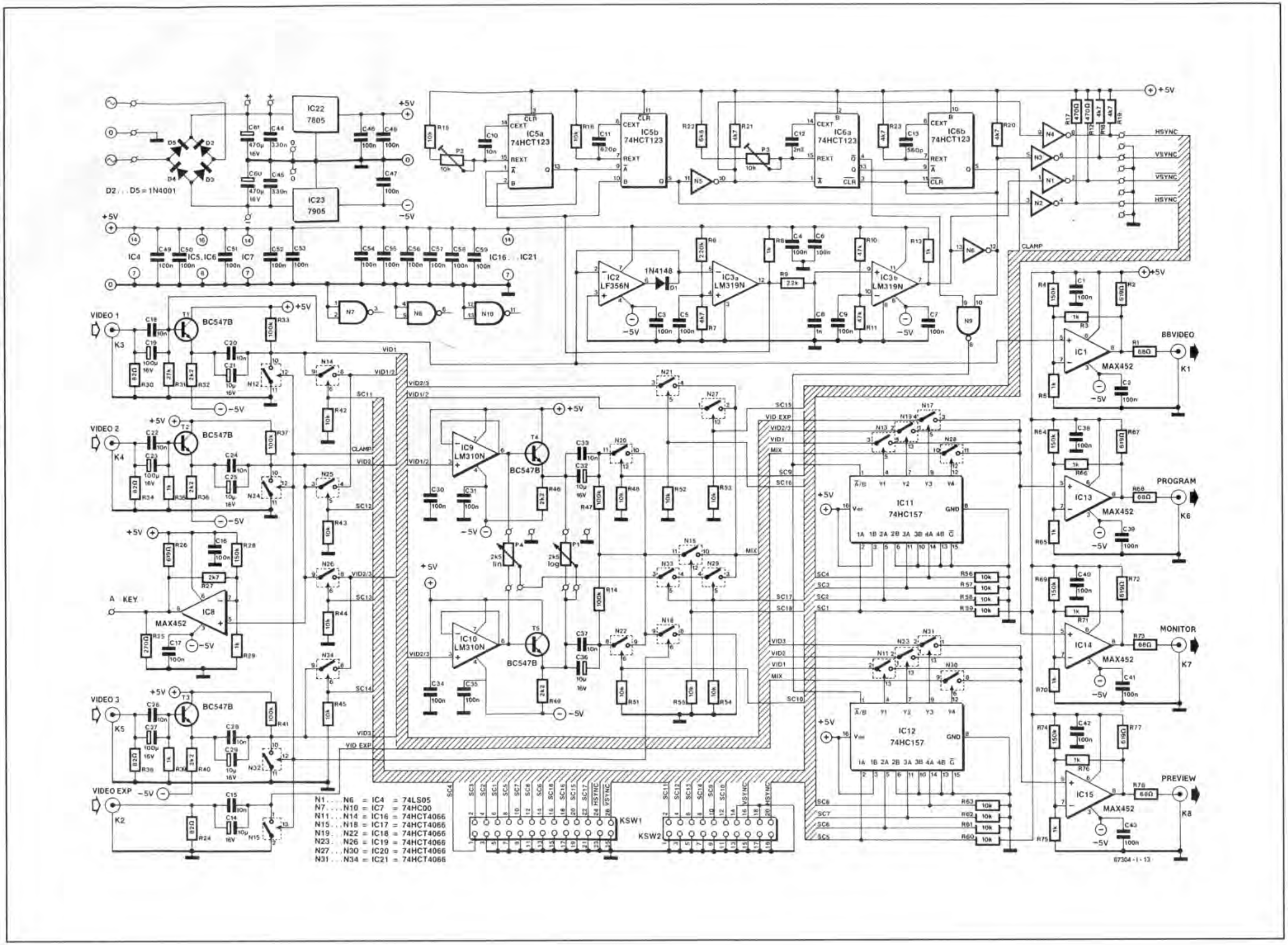


Fig. 3. Circuit diagram of the video switching module in the mixer.

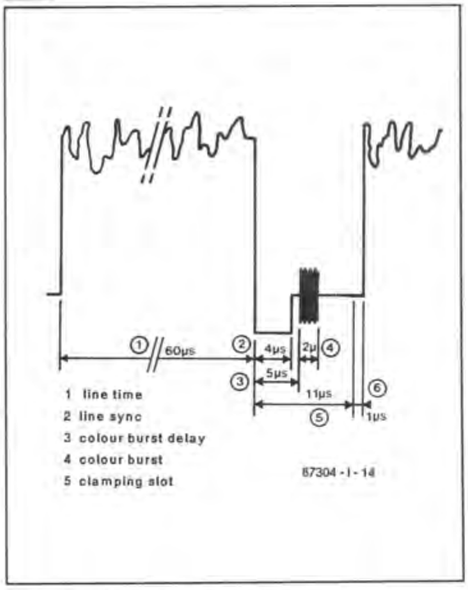


Fig. 4. Picture line timing.

weather maps.

Switching unit: the practical circuit

Although the circuit is fairly complex, the diagram in Fig. 3 gives a good insight into the operation of the video switching board.

The video signal applied to the VIDEO I input, socket K$_3$, serves to synchronize all other sources. Opamps IC$_2$, IC$_{3a}$ and IC$_{3b}$ form a synchronization separator. Circuit IC$_2$ clamps the input signal, while IC$_{3a}$ and the associated filter recover the line sync pulses. These trigger IC$_{5a}$, a monostable multivibrator (MMV), whose output pulses have a fixed length of 60 µs. These pulses keep a second MMV, IC$_{5b}$, from being started by interference during the picture line time, and ensure that a 4 µs horizontal sync pulse is generated by IC$_{5b}$ at the end of the line only. This gives a total time of 64 µs for the line content and the sync pulse, as shown in Fig. 4. The first picture information appears in the line 12 µs after the start of the line sync pulse. The third MMV, IC$_{6a}$, ensures that the line sync pulse and the colour burst recovered from video 1 are applied to all other video signals. This is achieved by NAND gate N$_9$ switching multiplexers IC$_{11}$ and IC$_{12}$ in a way that video-1 signals present during an 11 µs interval around the line sync pulse are passed to the output (by pre-selection on the $\overline{\mathrm{A}}$/B input).

Circuit IC$_{6b}$ generates a clamp pulse of approximately 1 µs before the start of the picture line content. The clamp pulse serves to define the absolute black level as a direct-voltage reference in the video signal.

The analogue circuitry on the video switching board starts at the left of the circuit diagram with three input buffers around transistors T$_1$, T$_2$ and T$_3$. These ensure that the video sources are terminated into the correct impedance, and further ensure sufficient drive for use at various points in the circuit. The inputs asa well as the outputs of the buffers are in series with parallel combinations of a solid (MKM) and an electrolytic capacitor to ensure a low reactance over a wide frequency range, which ensures that both the vertical and the horizontal sync pulses are passed undistorted. Each buffer output can be short-circuited by an electronic switch to give the required reference black level. The electronic switches are controlled by the clamping pulse.

There is a fair number of electronic switches between the buffers and the output. These switches are controlled from the keyboard circuit and select the two video signals that are to be mixed. The selected signals are first buffered for the benefit of two mixing effects.

First, the opamps used allow the signals to be mixed by potentiometer P$_4$. The mixed video signal at the wiper is passed through a series of electronic switches before it arrives at the output buffers, IC$_{13}$, IC$_{14}$ and IC$_{15}$.

Second, the amplifier that follows the mixer stage is used for the superimpose effect. Although the circuit around potentiometer P$_1$ looks similar to the mixer stage, it works altogether differently. Transistors T$_4$ and T$_5$ ensure sufficient buffering between the mixer and the superimpose stage, while potentiometer P$_1$ forms an adjustable short-circuit between the two video signals, which are mixed in a way that ensures that their brightest picture areas are passed to the output. Effectively, a relatively dark area in one picture is covered by a brighter one at the same location in the other picture. Switches N$_{20}$ and N$_{22}$ determine the video channel selection if the superimpose function is not used (P$_1$ set to maximum).

Circuits IC$_{11}$ and IC$_{12}$ have a number of functions related to the control of the video switching board. These functions will be reverted to in Part 2. For now, it is sufficient to say that control lines SC1 through SC8 are connected to switches that select the video signal that is to be fed to the output.

As will be seen in Part 2 of this article, the pattern generator on the modulation board controls lines SC15 through SC18 to enable two pictures to be mixed via an intermediate effect.

The circuit around opamp IC$_8$ raises the video signal at the VIDEO II input to a level suitable for driving the keying input on the modulation board.

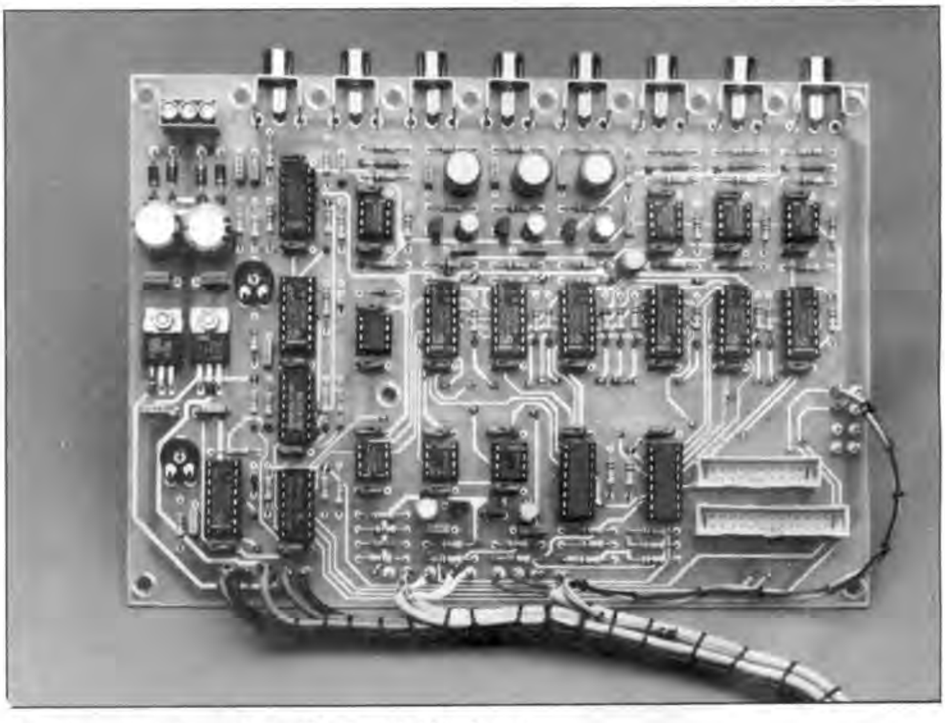
The power supply is quite simple. Every board has its own regulator, which takes the unregulated supply voltage from the central power supply. The video switching board has two local regulators, IC$_{22}$ and IC$_{23}$ to provide the symmetrical, regulated supply voltages of +5 V and – 5 V.

Construction

The printed-circuit board for this part of the project is a relatively large, double-sided and through-plated type, which is available ready-made. The component overlay shows that the board is fairly densely populated.

Use PCB-mount phono sockets for the video inputs and outputs as indicated on the component mounting plan. The synchronization signals, the supply voltage and the potentiometers are connected via solder pins. PCB headers KSW$_1$ and KSW$_2$ mate with IDC sockets fitted on short flat-cables that connect the video switching board to the keyboard unit and the modulator board.

Start the construction with fitting all connectors, solder pins and phono sockets. Then follow the passive components. Ample decoupling is provided by inex-



Completed prototype of the video switching board.

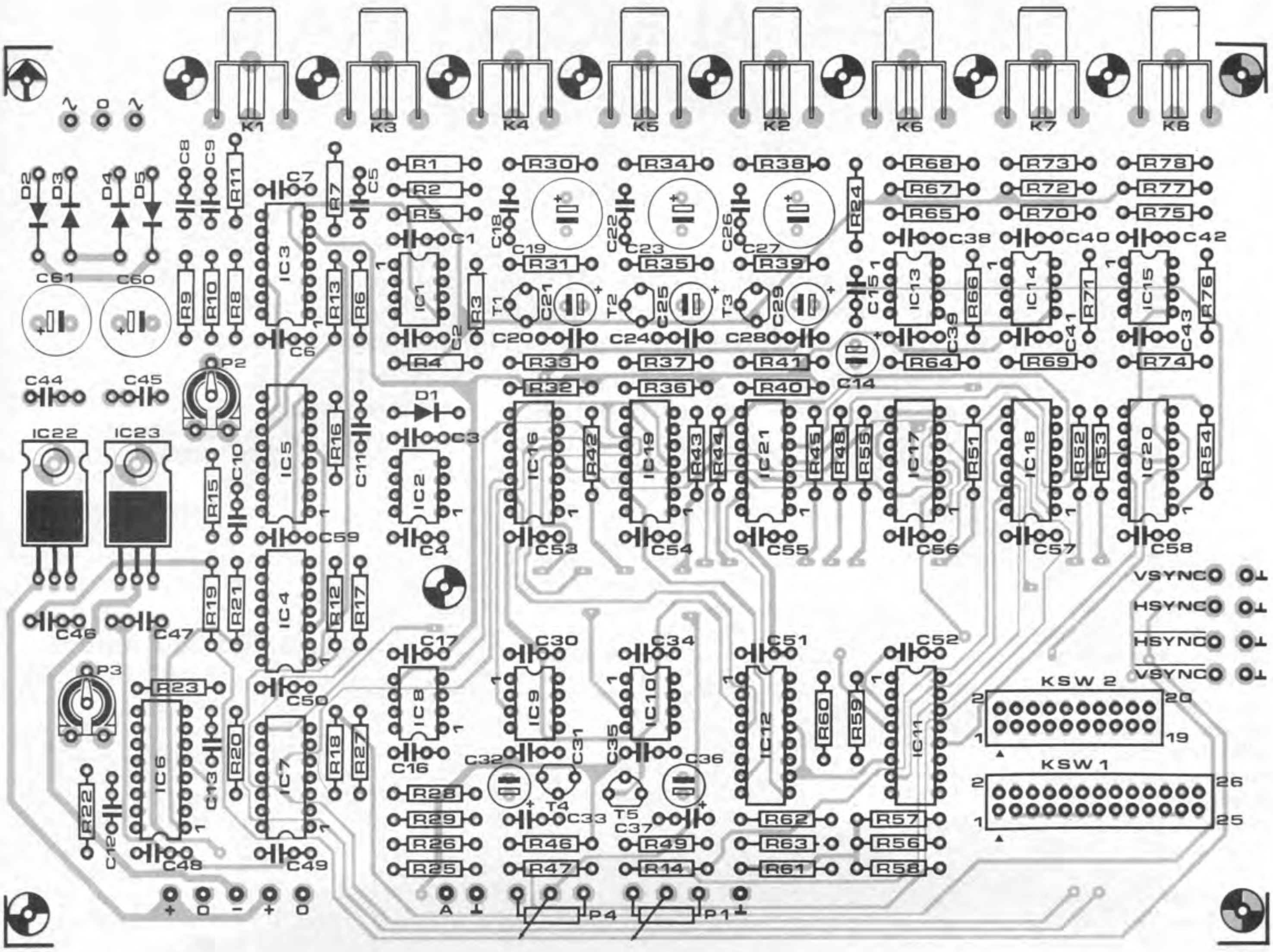


Fig. 5. Component mounting plan of the video switching board. The input and output cables are connected to PCB-mount phono sockets.

Parts list

Resistors:
R_1;R_{68};R_{73};R_{78} = 68Ω
R_2;R_{26};R_{67};R_{72};R_{77} = 619Ω (E96)
R_3;R_5;R_8;R_{13};R_{29};R_{35};R_{39};R_{65};R_{66};R_{70};
R_{71};R_{75};R_{76} = 1k0
R4;R_{28};R_{64};R_{69};R_{74} = 150k
R_6 = 220k
R_7;R_{18} – R_{21};R_{23} = 4k7
R9 = 22k
R_{10};R_{11} = 47k
R_{12};R_{17} = 470Ω
R_{32};R_{36};R_{40};R_{46};R_{49} = 2k2
R_{31} = 27k
R_{15};R_{16};R_{42} – R_{45};R_{48};R_{51} – R_{63} = 10k
R_{22} = 6k8
R_{24};R_{30};R_{34};R_{38} = 82Ω
R_{27} = 2k7
R_{14};R_{33};R_{37};R_{41};R_{47} = 100k
R_{25} = 270Ω
P_1 = 2k5 logarithmic potentiometer
P_2;P_3 = 10k preset H
P_4 = 2k5 linear potentiometer

Capacitors:
C_1 – C_7;C_9;C_{16};C_{17};C_{30};C_{31};C_{34};C_{35};
C_{38} – C_{43};C_{46} – C_{59} = 100n
C_8 = 1n0
C_{60};C_{61} = 470µ; 16 V; radial
C_{11} = 820p
C_{12} = 2n2
C_{13} = 560p
C_{10};C_{15};C_{18};C_{20};C_{22};C_{24};C_{26};C_{28};C_{33};
C_{37} = 10n
C_{19};C_{23};C_{27} = 100µ; 16 V; radial
C_{14};C_{21};C_{25};C_{29};C_{32};C_{36} = 10µ; 16 V; radial
C_{44};C_{45} = 330n

Semiconductors:
D_1 = 1N4148
D_2 – D_5 = 1N4001
IC_1;IC_8;IC_{13};IC_{14};IC_{15} = MAX452
IC_2 = LF356N
IC_3 = LM319N
IC_4 = 74LS05
IC_5;IC_6 = 74HCT123
IC_9;IC_{10} = LM310N
IC_{11};IC_{12} = 74HCT157
IC_{16} – IC_{21} = 74HCT4066
IC_{22} = 7805
IC_{23} = 7905
T_1 – T_5 = BC547B

Miscellaneous:
K_1 – K_8 = PCB-mount phono socket.
KSW_1 = 26-way pin header.
KSW_2 = 20-way pin header.
PCB Type 87304-1 (see Readers Services page).

pensive miniature 100 nF ceramic capacitors. IC sockets may be used, but are not strictly required. Note that many electrolytic capacitors are radial (PCB-mount) types to save board space.

Bend the terminals of the voltage regulators at right angles and secure these devices with a short M3 bolt. The regulators remain cool under normal conditions, and do not require heat-sinks.

Finally, check your work so far. Inspect the completed PCB for incorrectly fitted parts and short-circuits. The adjustment of P_2 and P_3 will be discussed in Part 4 of this article.

To be continued next month

THE DIGITAL MODEL TRAIN

PART 10 – RS232 INTERFACE

by T. Wigmore

The 9-way D-connector at the edge of the mother board offers the possibility of controlling the model railway by computer. This opens the way for fully automatic control of locomotives, turnouts (points), signals, protection of selected sections of the track, service schedules, simulated inertia of trains, combining locomotives for heavy goods trains, the switching of additional functions in rolling stock, and more.

The RS232 interface is compatible with the Märklin interface as far as standard instructions are concerned: the control of turnouts (points), signals and locomotives, and the calling for monitoring information. However, it offers many other facilities as well, such as requesting the state of locomotive controllers; the allocation of addresses to locomotive controllers; the disablement of keyboards and locomotive controllers as desired; the possibility of down-loading users' programs, and others. If manual control is not required, all keyboards and locomotive controllers may be omitted: all control instructions are then given via the interface. Mixed operation is also possible.

Originally, the RS232 standard was intended to couple a Data Communication Equipment (DCE, also called modem) and a Data Terminal Equipment (DTE), such as a computer. The standard is, unfortunately, abused by many manufacturers.

The Elektor Electronics Digital Train System is, strictly speaking, a DCE and, like the Märklin system, it uses three signal paths:

TxD: transmitted data – for data transport from the host computer to the EEDTS;
RxD: received data – for data transport from the EEDTS to the host computer;
CTS: clear to send – for advising the host computer that the EEDTS is ready for the next instruction.

Apart from these, an earth line is also required, so that the actual connexion cable must have at least four cores. A screen is not necessary. Recommended is four- or five-core flexible telephone cable. The length of the cable is of no consequence.

The cables shown in Fig. 62 will connect the EEDTS to most current computers that have an RS232 input. Some computers, such as the Commodore, require the signals to be inverted and their levels to be adapted to the TTL level; a suitable cable for these is shown in Fig. 63. The gates used here may be those as yet unused in IC9 on the mother board.

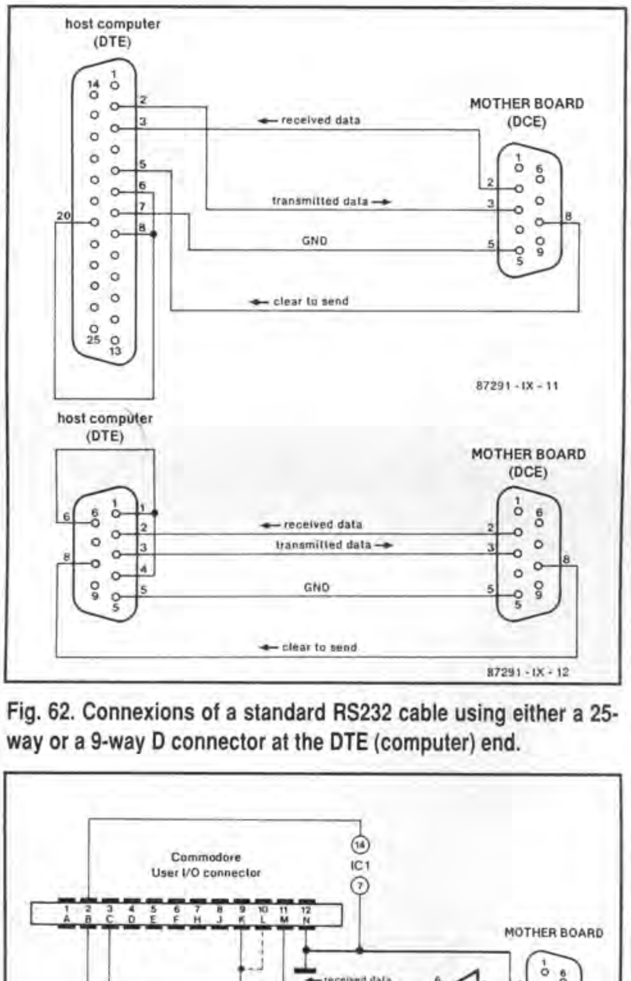


Fig. 62. Connexions of a standard RS232 cable using either a 25-way or a 9-way D connector at the DTE (computer) end.

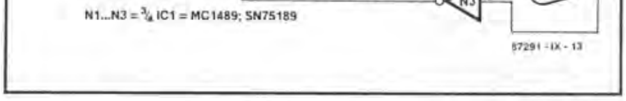


Fig. 63. When the EEDTS is to be connected to a Commodore, the signals must be inverted.

Baud rate and data format

On power-up, the interface is set for 2400 baud, eight data bits, no parity bit and two stop bits. Instructions must not be followed by a carriage return. The baud rate may be altered if needed: for instance, in noisy (electronically speaking) conditions or where a very long RS232 cable is used, 1200 baud (instruction <111>) is a more congenial operating frequency. For extensive tracks, a baud rate of 4800 (instruction <113>) is recommended. A reset, either by S3 or instruction <98> returns the operating frequency to 2400 baud.

The processing of an instruction received by the EEDTS is illustrated in Fig. 64. Basically, there are three types of instruction: 1-byte, 2-byte, and those that require the EEDTS to answer by data.

When a 1-byte or 2-byte command is received, CTS is deactuated for the short time the EEDTS requires to process the instruction. As soon as the stop bit is received, CTS becomes active again.

When an instruction is received that requires a response from the EEDTS, CTS is deactuated, and becomes active again only after the EEDTS has sent one or more data bytes to the DTE to indicate that the next instruction may be transmitted. This is half-duplex operation: full duplex working, that is, the simultaneous sending and receiving of data, is not possible.

The response time of the EEDTS depends on the type of instruction and, in the case of calling for monitoring information, on the numer of monitors used. The delay lies between 2 ms (one monitor) and 80 ms (62 monitors). This will be reverted

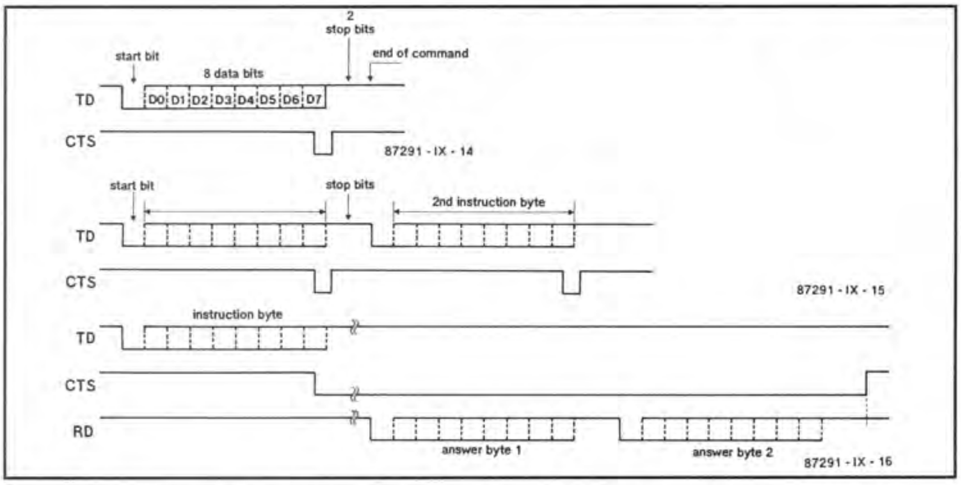


Fig. 64. The protocol for a 1-byte instruction (a); a 2-byte instruction (b); and a command that is followed by two answer-bytes (c).

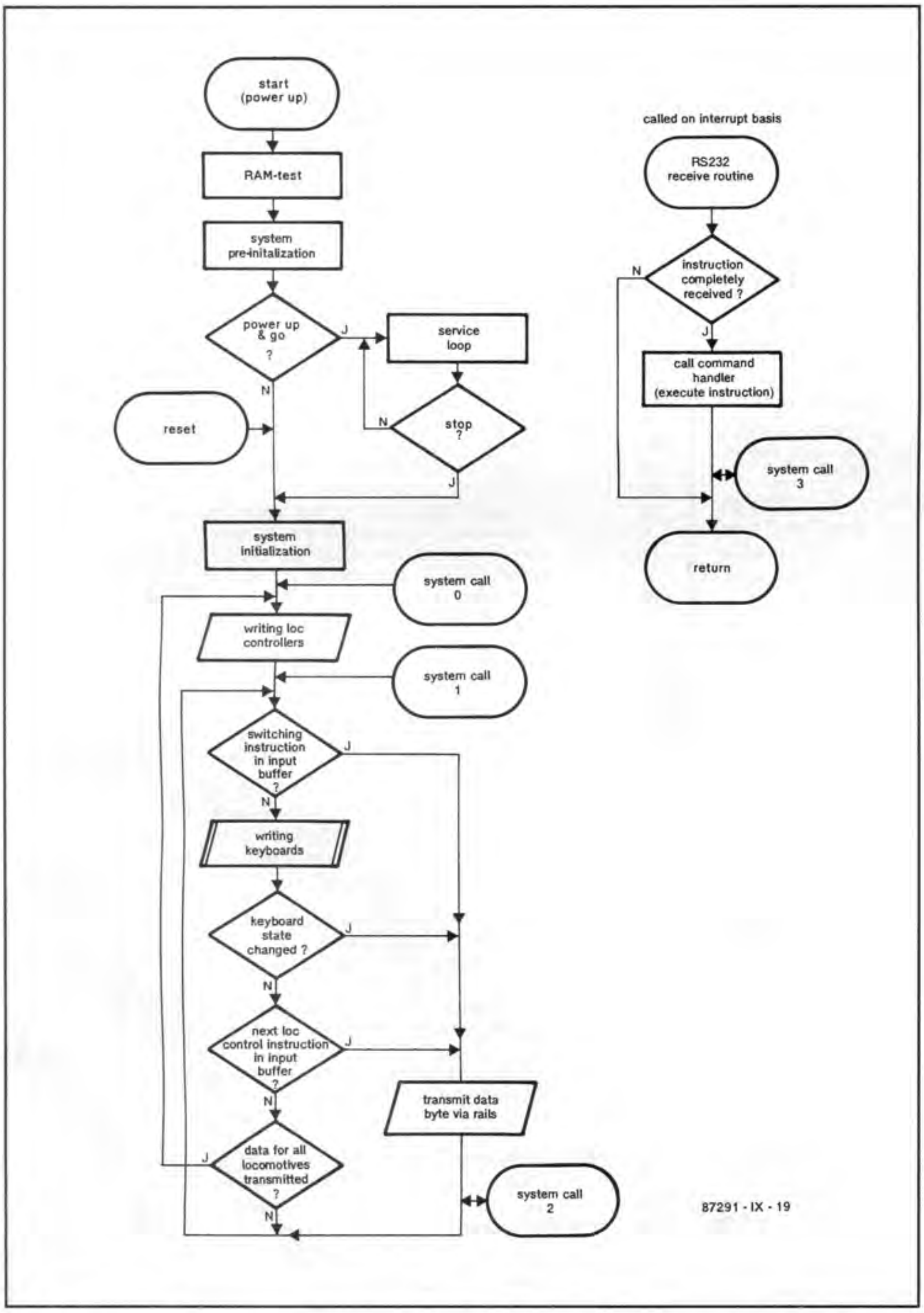


Fig. 65. Simplified flow diagram of the main loop in the system control program with indications where optional system programs may be called ((addressed).

to later.

EEDTS vs Märklin

All commands defined by Märklin have the same result in the EEDTS. Yet, there are several differences.

- In the stop mode, the Märklin system can receive only one instruction, whereas the EEDTS RS232 interface remains normally active. Monitor data can thus still be written. Switching instructions for turnouts (points) and signals may still be given but, since there is no voltage on the rails, they are retained in a buffer (up to 128 commands). When the buffer is full, CTS becomes inactive. As soon as the 'go' command is given, all switching instructions are executed in proper order.

- An energizing instruction for turnouts (points) or signals (<33>/<34>) must be followed in the Märklin system by a reset instruction (<32>). This is necessary to prevent the burning out of solenoids. In EEDTS, the reset instruction is generated automatically after a preset 'time out'.

- The numbering of turnouts (points) is slightly different between the two systems (see Table 7 in Part 9).Those that may be controlled via the RS232 interface are numbered 0–255.

- The monitor decoders in the Märklin system have 16 inputs, whereas those in the EEDTS have only eight. When the state of one monitor is requested, a program intended for the Märklin system expects a 2-byte reply. In the EEDTS a single byte would suffice, but there is then the likelihood that the program will wait (in vain) for the second byte. Therefore, the EEDTS provides Märklin simulation, in which it transmits the data of two units, i.e., two bytes, even if that of only one is called for. In other words, the monitor units are numbered in sets of two. If required, instruction <107> resets the system to the 'byte reply mode', in which the monitors are treated as single units again. After a reset or command <106>, the system is again in the 'word reply mode'.

System-status word and reset

The system status word, available with command <110>, contains information on the most relevant system data. After a reset or power-up, the system status word is 00H, which means that:

- the loc controllers and keyboards will be active as soon as the 'go' signal is given;
- there are no active switching instructions (system is in stop mode);
- the switching-instruction buffer is empty;

Instruction set

The instruction set is given in Table 8; all Märklin supported instructions are marked with an asterisk. All commands smaller than <80>, except <32>, are 2-byte instructions. The second byte of these consists of a loc address, a turnout (points) number and occasionally a time (the number indicated times 10 ms).

Instruction <32>, defined by Märklin as the turnout reset command, consists of only one byte and is active at the turnout number for which the latest switching command was given. This command is not used with the EEDTS.

Locomotive control

To actuate the additional function in Märklin loc decoders, the loc control instruction must be increased by 16. With EEDTS loc decoders the direction of travel is then reversed. The change-over instruction (<15> or, with actuated additional function, <31>) results in the EEDTS in the loc crawling backwards or forwards.

If a loc that is already controlled by a loc controller is also addressed via the RS232 interface, the controller is deactuated, since RS232 instructions have priority over others. Only after a loc enable instruction (<37>) or a system reset is the controller reactuated.

Turnout/signal control

Reset instruction <32> is not necessary. Command <33>, turnout straight on (signal green), means that the LED on the associated keyboard goes out. Instruction <34>, turnout turn-off (signal red) causes the LED to light.

When the status of one turnout is requested, the reply is one byte. This byte is false (0) if the turnout is set for straight on and true (255) if it is set for turn-off.

The standard turnout energizing delay after a reset or power-up is 250 ms. This delay may be altered to between 10 ms and 2.55 s by instruction <38>. The time is determined by the second byte ($t = n \times 10$ ms).

The position of turnouts and signals may be requested in groups of eight (commands 160–190 for several groups and 224–255 for a single group). Each group of eight gets a 1-byte reply. Each bit in this represents a turnout or signal. For instance, on command <161> (requesting first two groups), bit 0 of the first reply byte represents the state of turn-out 0, bit 7 that of turnout 7, bit 0 of the second reply byte the state of turnout 8 and bit 7 of the second reply byte that of turnout 15. If the position of turnouts (points) is requested that have not yet been energized, the reply by definition is 0 (straight on). Only after turnouts and signals have been energized at least once can their actual position be ascertained.

Programming loc controllers

Each locomotive controller may be given an address with instructions <48>–<63>, but only if the eight DIL switches at the relevant loc controller are off.

An address allocated to a loc controller via the RS232 interface will be erased if another address is set with the DIL switches.

Requesting loc controllers

The reply consists of a loc data byte and a loc address byte – see Fig. 66. The returned loc data contain information on speed, direction, whether an additional function is active or not, and the type of data format. Bit 4 is 1 if the function is active (Märklin data format) or if the loc is moving backwards (EEDTS data format).

If the controller is set for the Märklin data format, bit 5 will give information on the direction of travel (it is set if the controller is positioned for backward travel).

Bit 6 is set when the controller is set for EEDTS data format (loc data increased by 64). If a controller is not in use, the returned loc data is 255.

If the requested controller status is to be used for loc control information, bits 5 and 6 must be masked before the loc data is returned to the EEDTS.

The second reply byte is the loc address, 0–80. Bit 7 of this address gives information on its origin. For instance, if bit 7 is set (loc address increased by 128), the address was set via the RS232 interface.

System control

The differences between emergency stop <97>, reset <98> and stop all locs <99> are:

- the emergency stop removes the voltage from the rails and will thus immobilize the entire track; if fairly soon afterwards the 'go' command is given, all locs will continue at their previous speed;
- a reset is followed by a new system-initialization; again, the track will be at standstill; all settings made via the RS232 interface will be erased; in contrast to the situation after power-up, the actual turnout and signal states are retained.
- when all locs are halted, the voltage is not removed from the rails, although all moving locs are stopped; any locs that are

Locomotive control*		
0–14	[loc address]	loc control instruction; additional function not active
15	[loc address]	loc reverse instruction; additional function not active (only for Märklin decoders)
16–30	[loc address]	loc control instruction; additional function active for Märklin decoders; reverse travel with EEDTS decoders
31	[loc address]	switch-over instruction; additional function active (only with Märklin decoders]
Control of turnouts; calling for state of turnouts/monitors		
32		reset last turnout (points) (1-byte command)*
33	[no. of turnout]	set turnout for straight on*
34	[no. of turnout]	set turnout for turn-off*
35	[no. of turnout]	request status of single turnout; reply: 1 byte (0 or 255)
36	no. of contact)	request status of single monitor; reply: 1 byte (0 or 255)
37	[loc address]	loc enable command for one loc
38	[time]	set turnout delay (default = 250 ms)
39	[time]	set error time (default = 1 second)
40–47	[..]	unallocated 2-byte commands (not defined)
Programming of loc controller		
48–63	[address]	loc controller address instructions (no of controller = instruction – 46)
Future loc decoder switching instructions		
64–79	[address]	loc decoder switching instructions reserved by Märklin; four functions per decoder (not yet defined)
Loc controller request instructions		
80–95		request status of loc controllers (80 = controller 1) reply = 2 bytes [loc data][loc address]
System control instructions		
96		go*
97		stop (default at power-up)*
98		reset
99		stop all locs (no stop or reset)
100		enable keyboards (default)
101		disable keyboards
102		enable loc controllers (default)
103		disable loc controllers
104		write monitor status; normal mode (default)
105		write monitor status; differential mode
106		set monitor units to word-reply mode (Märklin emulation; default at power-up)
107		set monitor units to byte-reply mode
108		request number of monitor units
109		request number of locs in use
110		request system status (1-byte reply)
111		set baud rate to 1200
112		baud rate 2400 (default)
113		set baud rate to 4800
114–117		unallocated instructions
Down-load commands		
118		set down-load mode for files in binary format
119		set down-load mode for files in Intellec format
120–127		calls to user programs (error if no code is present at relevant RAM location)
Request instructions for status of a number of monitor units*		
128		do not reset monitors after writing
129–159		request state of a number of monitors (1–31)
Request instructions for state of several groups of 8 turnouts/signals		
160–191		request status of turnouts/signals in several groups of 8
Request instructions for status of a single monitor unit*		
192		reset monitor units after writing
193–223		request status of single monitor (no. = command – 192)
Request instruction for status of turnouts/signals, single group of 8		
224–255		request status of any group of 8 turnouts or signals
Definition of parameters:		
[loc address]	=0–80	
[no. of turnout]	=0–255	
[no. of monitor]	= 0–255	
[time]	= 0–255 × 10 ms (0–2.55 s)	

Table 8. Definitions of RS232 instructions.

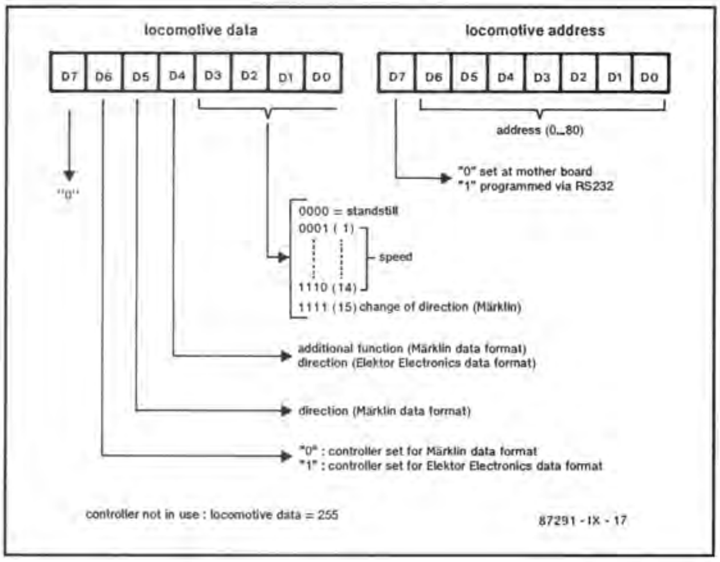

locomotive data
locomotive address
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0
address (0...80)
"0" set at mother board
"1" programmed via RS232
"0"
0000 = standstill
0001 (1)
speed
1110 (14)
1111 (15) change of direction (Märklin)
additional function (Märklin data format)
direction (Elektor Electronics data format)
direction (Märklin data format)
"0" : controller set for Märklin data format
"1" : controller set for Elektor Electronics data format
controller not in use : locomotive data = 255
87291 - IX - 17

Fig. 67. Definition of the returned data when a loc controller is requested.

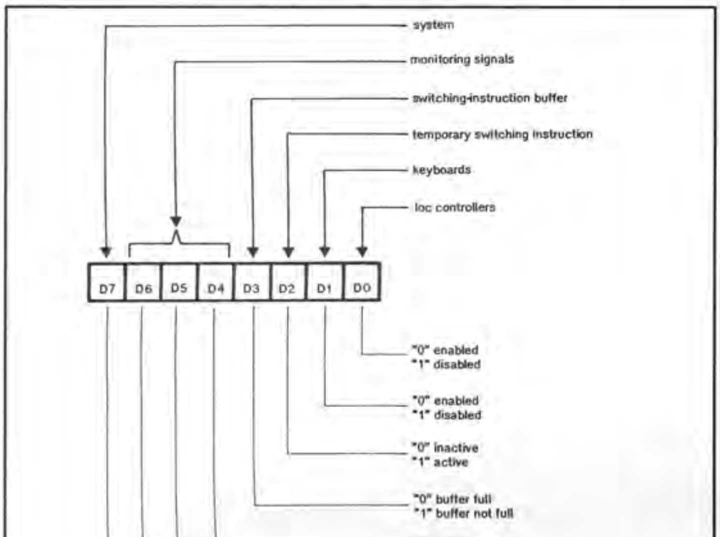


Fig. 68. Construction of system-status word: at power-up, it is 00H.

under the command of a controller will resume their previous speed; this may be prevented by preceding the stop all locs command by the loc controller disable instruction, <103>.

Disabling controllers and keyboards may be useful in fully automatic operation. When the keyboards are disabled, the yellow LED on the mother board lights.

Monitor signals

Instructions <106> and <107> enable the requesting of data from a single unit or from two units respectively. After power-up or a reset, the EEDTS is in the word-reply mode.

Monitor contacts are reset immediately they are written, unless the reset is disabled by <128>. The reset may be enabled again by <192>.

Normally, a monitor contact is written as a 1 if it is active. It is, however, possible with <105> to switch over to the differential mode, in which the contact is read as 1 only if it has altered. This makes it easy to see where something has happened.
The number of monitor units in use may be requested with instruction <108>.

Examples of programming

Since the program occupies some 200 Kbyte, it can not be given here. To help you on your way, however, some examples are given on how to actuate the basic functions of the EEDTS from GWBASIC (as supplied with every PC). If you use another variant of BASIC, or a different machine, or a different language, consult the associated handbooks.

The programming examples are fairly basic and they should therefore be treated as direction indicators only.

Before each command, the CTS line should be tested to see whether the system is ready to receive commands. This check is, however, often carried out by the system and also, for instance, by the GWBASIC interpreter. If instructions are attempted to be sent while the CTS line is inactive, the BASIC interpreter will give an I/O time out error. Generally, however, the processing of the commands is so rapid that no problems should be encountered.

INITIALIZING THE RS232 INPUT

```
10 REM closes all open files
20 CLOSE
30 REM open COM1(RS232)
    2400 Baud, no parity, 8 data
    bits
40 REM 2 stop bits as file 1
50 OPEN “COM1:2400,N,8,2”
    AS#1
```

LOCOMOTIVE CONTROL COMMAND

```
100 INPUT “give loc control com-
    mand (0–31)”COMMAND
110 INPUT “give loc address
    (≤80)” ADDRESS
120 PRINT #1,CHR$
    (COMMAND)
130 PRINT #1,CHR$
    (ADDRESS)
```

Note that the PRINT instructions in lines 120 and 130 must be closed by “;” to indicate that no carriage return must follow.

TURNOUTS CONTROL COMMAND

```
200 INPUT “give no. of turnout
    (0–255)” TURNOUTS
210 INPUT “position (0 =
    straight on; 1 = turn off”,
    POSITION
230 IF POSITION = 0 PRINT
    #1,CHR$(33); OTHERWISE
    PRINT#1,CHR$(34)
240 PRINT #1,CHR$
    (TURNOUT)
```

SETTING TURNOUTS DELAY

(default = 0.25 s)

```
300 INPUT “new turnouts delay
    (0–255* 10 ms)” TIME
310 PRINT #1,CHR$(38)
320 PRINT #1,CHR$(TIME)
```

REQUESTING STATE OF MONITORS

(193–223)

```
400 INPUT “required unit/group
    number (1–31)” UNITNR
410 PRINT #1,CHR$
    (UNITNR +192)
420 A$=INPUT$(2,#1)
430 PRINT “unit”
    (UNITNR–1)*2 +1 =
    “ASC(LEFT$(A$,1))
440 PRINT “unit”
    (UNITNR–1)*2 +2”
    “ASC(RIGHT$(A$,1))
```

In this example it is assumed that the system is in the word-reply mode; the monitor units are written as pairs. The digit ‘2’ in line 420 shows that a reply of 2 bytes is expected. These reply bytes are separated in lines 430 and 440. In the byte-reply mode, line 420 becomes:

```
420 A$=INPUT$(1,#1)
```

and line 440 is omitted.

REQUESTING STATUS OF A SINGLE MONITOR

```
500 INPUT “call monitor unit
    (0–255)” CONTACT
510 PRINT #1,CHR$(36)
520 PRINT #1,CHR$
    (CONTACT)
530 A$=INPUT$(1,#1)
540 CONTACT STATE=ASC(A$)
550 IF CONTACT STATE=0,
    B$=“not active” OTHERWISE
    B$=“(was) active”
560 PRINT “monitor”; CONTACT
    “is”; B$
```

REQUESTING STATUS OF TURNOUTS

The state of turnouts is requested in the same way as that of monitors with the exception that only a 1-byte reply follows a group of eight turnouts.

ALLOCATING A LOC ADDRESS TO A LOC CONTROLLER

```
600 INPUT “address setting in-
    struction for loc controller
    (1–16)”,REGNR
610 INPUT “required loc address
    (≤80)”,ADDRESS
620 PRINT
    #1,CHR$(REGNR + 47)
630 PRINT #1,CHR$(ADDRESS)
```

REQUESTING STATUS OF LOC CONTROLLER

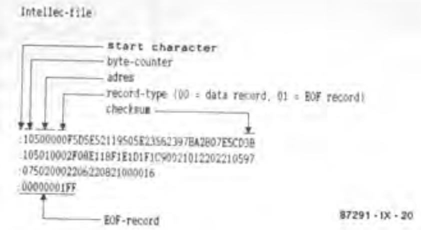
```
700 INPUT “request instruction
    for loc controller (1–16)”,
    REGNR
710 PRINT
720 PRINT
    #1,CHR$(REGNR+79)
730 A$=INPUT$(2,#1)
740PRINT “locdata=”
    ASC(LEFT$(AS,1))
750 PRINT “loc address=”
    ASC(RIGHT$(A$,1))
```

In the last example, the reply also consists of two bytes (line 730) which are separated in lines 740 and 750 into the address for which the controller is set and the associated controller status (loc data).

RAM address	Call	Misc
4800H	system call 1	)
4900H	system call 2	) see Fig. 65
4A00H	system call 3	)
4B00H	system call 0	)
		instruction:
5000H	user call 0	<120>
5100H	user call 1	<121>
5200H	user call 2	<122>
5300H	user call 3	<123>
5400H	user call 4	<124>
5500H	user call 5	<125>
5600H	user call 6	<126>
5700H	user call 7	<127>

Table 9. RAM addresses available for down-loading.

```
                                ;**************************************************
                                ;turnouts and signals preset routine
                                ;may be called with command <120>
                                ;**************************************************

             082F               WIS_COM:  EQU  082FH      ;start address of system routine for
                                                          ;conversion of switch commands
                                                          ;and turnout numbers, and storage of
                                                          ;result in buffer

      5000                                ORG  5000H      ;RAM-address 5000 is called
                                                          ;with command <120>

      5000   F5                           PUSH AF         ;save registers
      5001   D5                           PUSH DE
      5002   E5                           PUSH HL
      5003   21 19 50                     LD   HL,WIS_TBL
      5006   5E                 NXT_COM:  LD   E,(HL)     ;copy turnout number and command
      5007   23                           INC  HL         ;from table to register DE
      5008   56                           LD   D,(HL)
      5009   23                           INC  HL
      500A   97                           SUB  A          ;A:=0
      500B   BA                           CP   D          ;no switch command
      500C   28 07                        JR   Z,WIS_END  ;= end of table
      500E   E5                           PUSH HL
      500F   CD 2F 08                     CALL WIS_COM    ;convert turnout number and
                                                          ;turnout command
      5012   E1                           POP  HL
      5013   18 F1                        JR   NXT_COM

      5015   E1                 WIS_END:  POP  HL         ;restore registers
      5016   D1                           POP  DE
      5017   F1                           POP  AF
      5018   C9                           RET

                                          ;switching commands table
                                          ;<turnout number><command>
                                          ;end of table = <0><0>
                                          ;max. 128 commands in table
      5019   00 21              WIS_TBL:  BYTE 0,33       ;turnout 0, straight on
      501B   01 22                        BYTE 1,34       ;turnout 1, divert
      501D   02 21                        BYTE 2,33       ;turnout 2, straight on
      501F   05 22                        BYTE 5,34       ;turnout 5, divert
      5021   06 22                        BYTE 6,34       ;turnout 6, divert
      5023   08 21                        BYTE 8,33       ;turnout 8, straight on
                                                          ;table may be extended
                                                          ;to requirement
      5025   00 00                        BYTE 0,0        ;closes table

      5027                                END


        Lines Assembled :  51              Assembly Errors :  0
```



```
:10500000F5D5E52119505E23562397BA2807E5CD3B
:105010002F08E118F1E1D1F1C90021012202210597
:075020002206220821000016
:00000001FF
```

Fig. 68. Example of a programme in assembler to preset a number of turnouts (points) with instruction <120>. Underneath the associated down-load file in Intellec format.

- the monitor units are in normal mode and will be reset automatically after writing and the word reply mode is active;
- the stop-status is active (no voltage on the rails).

On a reset via S3 or instruction <98>, apart from the above default settings, the following will happen:

- all loc controllers are enabled, including those that are active at loc addresses where previously an RS232 command was active;
- the baud rate is set at 2400 baud;
- the energizing delay for turnouts (points) is set to 0.25 s;
- the loc addresses set via the RS232 at the loc controllers become inactive;
- all down-loaded user programs will be erased.

The situation after a reset is thus almost the same as after power-up; the only difference is that the prevailing positions of turnouts (points) and signals are retained.

Error LED

The error LED will light when the EEDTS receives an incompatible instruction. Examples of such commands, which are ignored by the system, are:

- a non-existent loc address;
- an attempt at addressing a loc controller that has already been set to a different address;
- calling for the status of a non-connected monitor;
- a non-defined instruction;
- addressing a non-down-loaded user program;
- the start bit on the serial channel is shorter than expected for the set baud rate (may also be a spurious pulse).

The diode will light for one second, unless this duration has been altered via command <39>, but in three situations it will light permanently:

- when during the auto test an error is detected in the RAM (when IC14 should be replaced);
- when a non-existent loc address has been set in the diode matrix (which thus should be undone);
- when a transmission error is detected during the down-loading of a file (possibly caused by a wrong baud rate – reset and try again).

Down-load mode

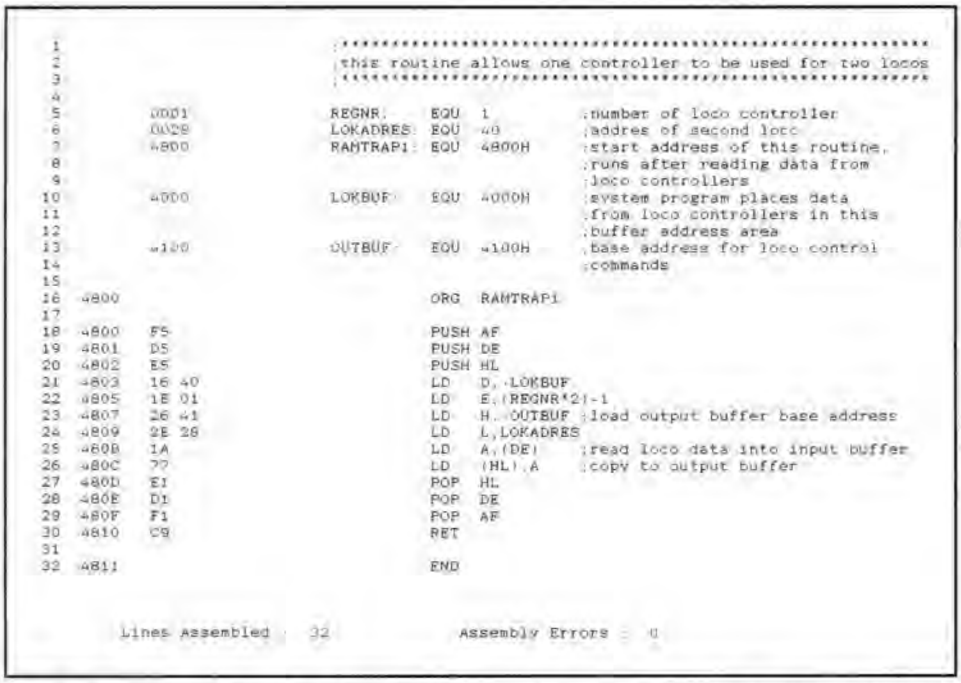
The down-load mode enables user programs to be loaded from the host computer into the RAM of the EEDTS in Z80 machine language.

Basically there are programs that are addressed by separate commands and programs that are addressed (called) cyclically by the EEDTS. Figure 65 shows where in the control program the EEDTS executes such a call to a possible user program.

Two instructions are available for down-loading: <118> and <119>.

Instruction <118> sets the binary down-load mode, in which the EEDTS expects a binary down-load file preceded by two 2-byte RAM addresses (high-order address part first). These addresses determine where the first and last byte will be written and must agree with the number of transmitted data bytes because each subsequent byte will be interpreted as a normal instruction.

Command <119> sets the EEDTS to a mode in which it is possible to down-load files in Intel"s Intellec-8 format. Most assemblers are able to create an output file in this format. Such a (strictly speaking ASCII) file contains apart from data also all necessary address information and a checksum for each block of 256 bytes. If through this checksum a transmission



```
                                  ;**************************************************************
                                  ;this routine allows one controller to be used for two locos
                                  ;**************************************************************

            0001                  REGNR:      EQU  1             ;number of loco controller
            0028                  LOKADRES:   EQU  40            ;addres of second loco
            4800                  RAMTRAP1:   EQU  4800H         ;start address of this routine,
                                                                 ;runs after reading data from
                                                                 ;loco controllers
            4000                  LOKBUF:     EQU  4000H         ;system program places data
                                                                 ;from loco controllers in this
                                                                 ;buffer address area
            4100                  OUTBUF:     EQU  4100H         ;base address for loco control
                                                                 ;commands

      4800                                    ORG  RAMTRAP1

      4800  F5                                PUSH AF
      4801  D5                                PUSH DE
      4802  E5                                PUSH HL
      4803  16 40                             LD   D, LOKBUF
      4805  1E 01                             LD   E,(REGNR*2)-1
      4807  26 41                             LD   H, OUTBUF ;load output buffer base address
      4809  2E 28                             LD   L,LOKADRES
      480B  1A                                LD   A,(DE)      ;read loco data into input buffer
      480C  77                                LD   (HL),A      ;copy to output buffer
      480D  E1                                POP  HL
      480E  D1                                POP  DE
      480F  F1                                POP  AF
      4810  C9                                RET

      4811                                    END


         Lines Assembled :  32              Assembly Errors :  0
```

Fig. 69. Assembler program to be down-loaded to enable two locomotives to be controlled via one controller.

error is detected, the EEDTS goes into the stop mode and the error LED lights permanently. The system must then be reset by S3, after which the down-loading may be restarted.

Table 9 shows where in the RAM data may be down-loaded. However, the system does not verify whether the down-loading really takes place at these addresses: in principle, writing may take place anywhere in the RAM, even in those parts that are used by the system.

During down-loading, the main program is interrupted and the system is in the stop mode to prevent the addressing of a routine that is to be called cyclically before its down-loading has been completed. In the down-load mode, the yellow LED flashes in a 2 Hz rhythm.

The down-loading is initiated by the command copy <file name> com1:. After the down-loading has been completed, the LED will stop flashing; the 'go' command must then be given to reactuate the system.

Some examples

Two examples will be given to illustrate what has been said so far.

The first is a routine (see Fig. 68) to set a number of turnouts (points) or signals (max. 128) to a given position.

Since this routine starts at address 5000H, it is actuated by command <120>. In the routine, the switching commands for the relevant turnouts and signals are first copied to register set DE and then, in system routine WIS COM, to the switching command buffer. The main program of the system will ensure that these switching commands are executed in due course. By adapting the data lines at the end of the routine, anyone is able to define his own presets for turnouts (points).

Each switching command consists of two bytes: the number of the turnout or signal followed by the switching command: <33> for straight on and <34> for turning off. After command <34> the row must be closed by 0000H.

The second example (see Fig. 69) is a routine that is addressed cyclically every time the state of the loc controllers is written. In this program, the data that was written by the loc controller is copied to the location for loc address 40 in the output buffer. This means that loc controller 1 will be active on the locomotive for which controller 1 has been set as well as on the locomotive with address 40. These locomotives are then coupled via software and may be controlled via one controller. This is, for instance, useful when a heavy goods train can not be pulled by one locomotive.

The coupled control is undone by sending a single byte (C9, the Z80 return command) to the start address in the RAM of the present routine. It may also be done by resetting the system.

In general, the original contents of all registers used in a user program should be stored in the stack from the beginning. At the end of the user routine, the contents of these registers must, of course, be recovered.

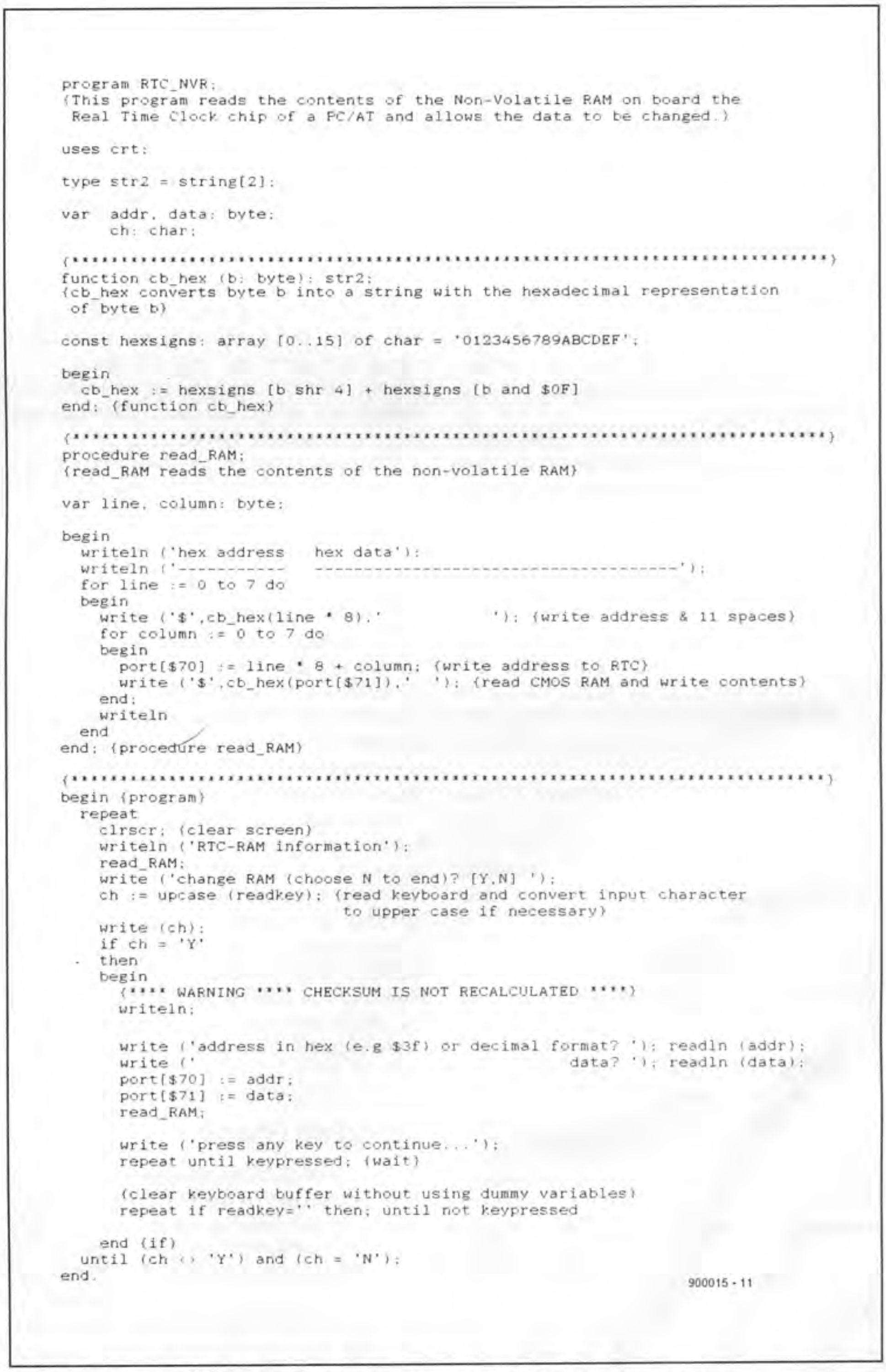
Listing on floppy

In the development of user programs a good knowledge of the EEDTS control program is indispensable. Unfortunately, this program can not be given in this article, since, together with the HEX codes, an extensive commentary, and cross-references, it occupies some 200 Kbyte. It is, however, available through the Readers' Services on a 5.25-inch, 360 Kbyte floppy under reference ESS-109.

CMOS RAM CONTROL FOR PC-AT

from an idea by H. van den Bosch

The program listed here is written in Turbo Pascal to compile a small program, RTC-NVR.EXE, that enables owners of PC/ATs or any other IBM PC compatible fitted with a real-time clock (RTC) circuit to examine and, if necessary, change the contents of the non-volatile CMOS RAM that holds the time and date, as well as system configuration ('set-up') information.



```
program RTC_NVR;
(This program reads the contents of the Non-Volatile RAM on board the
 Real Time Clock chip of a PC/AT and allows the data to be changed.)

uses crt;

type str2 = string[2];

var  addr, data: byte;
     ch: char;

{*************************************************************************}
function cb_hex (b: byte): str2;
{cb_hex converts byte b into a string with the hexadecimal representation
 of byte b}

const hexsigns: array [0..15] of char = '0123456789ABCDEF';

begin
  cb_hex := hexsigns [b shr 4] + hexsigns [b and $0F]
end; {function cb_hex}

{*************************************************************************}
procedure read_RAM;
{read_RAM reads the contents of the non-volatile RAM}

var line, column: byte;

begin
  writeln ('hex address   hex data');
  writeln ('-----------   -------------------------------------');
  for line := 0 to 7 do
  begin
    write ('$',cb_hex(line * 8),'           '); {write address & 11 spaces}
    for column := 0 to 7 do
    begin
      port[$70] := line * 8 + column; {write address to RTC}
      write ('$',cb_hex(port[$71]),'  '); {read CMOS RAM and write contents}
    end;
    writeln
  end
end; {procedure read_RAM}

{*************************************************************************}
begin {program}
  repeat
    clrscr; {clear screen}
    writeln ('RTC-RAM information');
    read_RAM;
    write ('change RAM (choose N to end)? [Y,N] ');
    ch := upcase (readkey); {read keyboard and convert input character
                             to upper case if necessary}
    write (ch);
    if ch = 'Y'
    then
    begin
      {**** WARNING **** CHECKSUM IS NOT RECALCULATED ****}
      writeln;

      write ('address in hex (e.g $3f) or decimal format? '); readln (addr);
      write ('                                       data? '); readln (data);
      port[$70] := addr;
      port[$71] := data;
      read_RAM;

      write ('press any key to continue...');
      repeat until keypressed; {wait}

      {clear keyboard buffer without using dummy variables}
      repeat if readkey='' then; until not keypressed

    end {if}
  until (ch <> 'Y') and (ch = 'N');
end.
```

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Fig. 1. **Listing of the Turbo-Pascal program used to compile RTC-NVR.EXE.**

Any PC-AT or compatible has a 64-byte CMOS RAM and a real-time clock powered by a re-chargeable battery. In the standard IBM PC-AT (who still has such an oldie?), the two functions are combined in a Motorola Type MC146818 integrated circuit on the motherboard. In the latest generation of AT compatibles, however, the RTC and the RAM are usually contained in one of the VLSI components that form part of the manufacturer's chip set. In general, owners of a PC-AT need not worry about the exact location of the RTC and non-volatile RAM: the only thing that counts is that the two can be found at the right memory address. Fortunately, most clone manufacturers keep to the I/O address assignment drawn up by IBM.

A timed surprise?

To be informed by the computer that the set-up information is lost owing to a system malfunction or an exhausted battery is at best a temporary nuisance and at worst the beginning of a real hassle to unearth notes made a long time ago on hard disk drive parameters, RAM bank configurations, wait states, and so on.

Although the required information can be refurnished relatively quickly with the aid of the set-up utility provided with the computer, it is useful in many cases to have the RTC/RAM contents available on paper in the form of a hex dump.

The author recently suffered a malfunction in the power supply of his PC-AT compatible. After this had been repaired, the machine on being switched on reported a hard disk controller fault, and could not be made to boot from drive C: as usual. The previously written utility RTC-NVR.EXE was available on floppy disk, however, and on being run indicated that the two checksum bytes at addresses 2E and 2F (see Tables 1 and 2) had been corrupted, probably as a result of the power supply malfunction. The bytes were recalculated, modified, and the machine performed a normal boot-up operation.

Document your settings

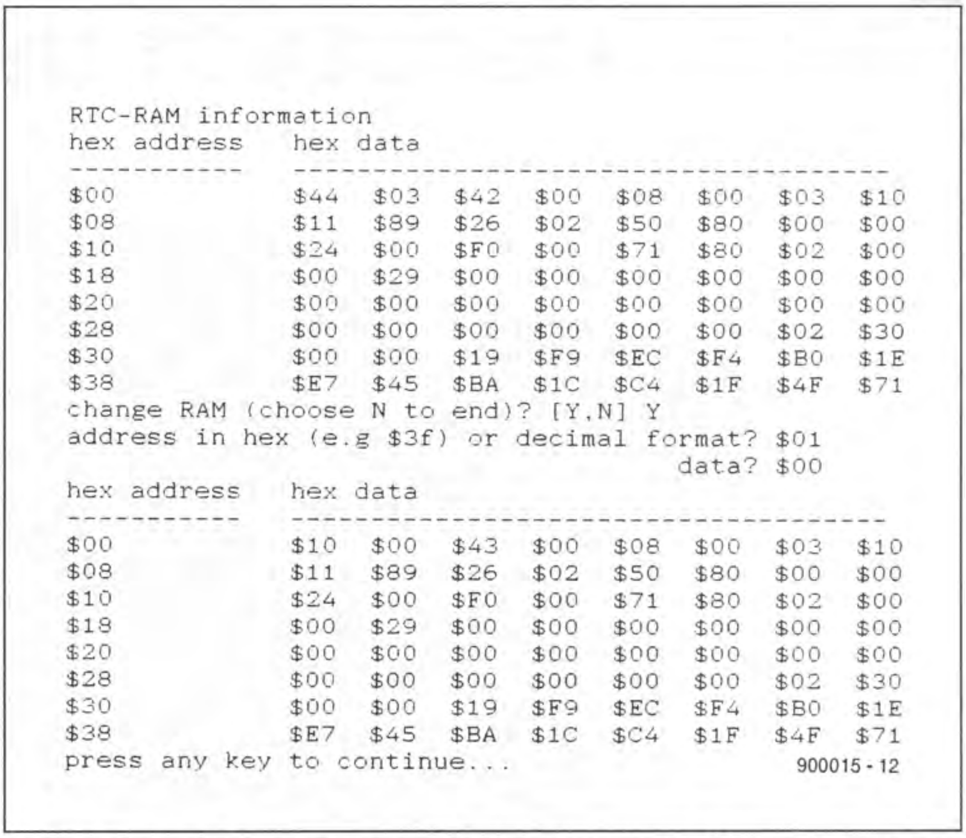
The listing in Fig. 1 is typed into Turbo Pascal and then compiled to obtain the required .EXE file. Routines 'upcase' and

Byte	Function	Address
0	Seconds	00
1	Second Alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Day of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

Table 2. Real-time clock addresses.

Addresses	Description
00–0D	Real-time clock information
OE	Diagnostic status byte
0F	Shut-down status byte
10	Diskette drive type byte (drives A and B)
11	Reserved
12	Fixed disk drive type (drives C and D)
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19–2D	Reserved
2E–2F	2-byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Date century byte
33	Information flags (set during power-on)
34–3F	Reserved

Table 1. CMOS RAM address map.



```
RTC-RAM information
hex address    hex data
-----------    ---------------------------------------
$00            $44  $03  $42  $00  $08  $00  $03  $10
$08            $11  $89  $26  $02  $50  $80  $00  $00
$10            $24  $00  $F0  $00  $71  $80  $02  $00
$18            $00  $29  $00  $00  $00  $00  $00  $00
$20            $00  $00  $00  $00  $00  $00  $00  $00
$28            $00  $00  $00  $00  $00  $00  $02  $30
$30            $00  $00  $19  $F9  $EC  $F4  $B0  $1E
$38            $E7  $45  $BA  $1C  $C4  $1F  $4F  $71
change RAM (choose N to end)? [Y,N] Y
address in hex (e.g $3f) or decimal format? $01
                                      data? $00
hex address    hex data
-----------    ---------------------------------------
$00            $10  $00  $43  $00  $08  $00  $03  $10
$08            $11  $89  $26  $02  $50  $80  $00  $00
$10            $24  $00  $F0  $00  $71  $80  $02  $00
$18            $00  $29  $00  $00  $00  $00  $00  $00
$20            $00  $00  $00  $00  $00  $00  $00  $00
$28            $00  $00  $00  $00  $00  $00  $02  $30
$30            $00  $00  $19  $F9  $EC  $F4  $B0  $1E
$38            $E7  $45  $BA  $1C  $C4  $1F  $4F  $71
press any key to continue...
```

900015 - 12

Fig. 2. Print-out to illustrate the operation of the non-volatile RAM utility. The computer used for this test was a NEAT-286/4 AT compatibie. By studying the dump carefully, you can see when this article was written, and how many seconds it took to modify the data at address $01, the seconds alarm in the RTC.

'readkey' are procedures resident in Turbo Pascal. Data is read via I/O port 71, while port 70 serves to address the 64 bytes. An example of the output of the program is shown in Fig. 2. The RAM addresses may be entered in hexadecimal (preceded by a $ sign) or in decimal.

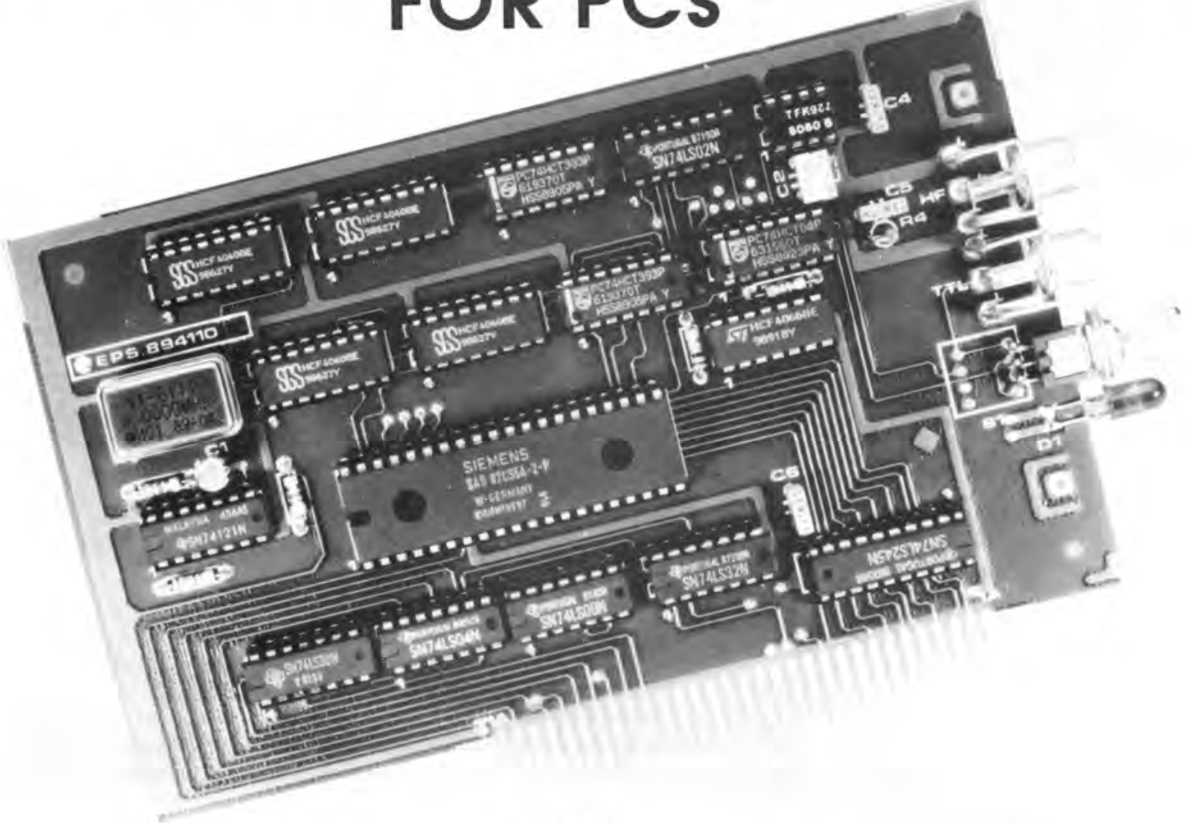
The program is also suitable for the popular Amstrad PC1640, and should also work on PC-XTs equipped with a multi-I/O card, although this has not been tested.

Finally, be sure to copy RTC-NVR.EXE to a floppy disk if you have compiled the program on hard disk. Make the floppy bootable by adding CONFIG.SYS, COMMAND.COM and an AUTOEXEC.BAT file that calls up RTC-NVR.EXE.

Byte(s)	Usage	Default
0–9	RTC time and date parameters	--
10	RTC control register A	070H
11	RTC control register B	002H
12	RTC control register C	--
13	RTC control register D	--
14–19	Time and date when machine was last used	--
20	User RAM checksum	--
21-22	Enter key translation token	01C0DH
23-24	Forward key translation token	02207H
25-26	Joystick fire button 1 translation token	0FFFFH
27-28	Joystick fire button 2 translation token	0FFFFH
29-30	Mouse button 1 translation token	0FFFFH
31-32	Mouse button 2 translation token	0FFFFH
33	Mouse X direction scaling factor	00AH
34	Mouse Y direction scaling factor	00AH
35	Initial video mode and drive count	020H
36	Initial video character attributes	007H
37	Size of RAM disk in 2-Kbyte blocks	000H

Table 3. Amstrad PC1640 non-volatile RAM address map.

1 GHz FREQUENCY METER CARD FOR PCs



H. Kolter

This plug-in card for IBM PC-XT/AT and compatibles forms a cost-efficient alternative to a stand-alone frequency meter. Simple to build and program, the card has a TTL input as well as a prescaler input with high sensitivity that can handle frequencies up to 1 GHz.

The signals on the expansion slots of an IBM PC or compatible machine form the starting point for the design of any extension card for this type of computer. The hardware that arranges the data flow and addressing must be laid out carefully to meet the technical requirements drawn up during the design stages. In practice, the eight bidirectional datalines between the extension card and the motherboard must be buffered to prevent the drive capacity of the CPU and associated peripheral chips being exceeded at the risk of permanent damage to the computer. The next requirement is that the extension circuit must occupy a carefully selected address range that can be accessed by the CPU in accordance with the I/O (input/output) map defined by IBM. Hence, the address range occupied by the extension card must be unique in the computer system to avoid I/O contention problems.

The frequency meter card presented here has a Type 8255 PPI (Programmable Peripheral Interface) to meet the above requirements as regards buffering and address decoding. All control of counter and clock circuits on the extension card is arranged by the CPU via the three data registers and one control register contained in the 8255 PPI.

Frequency measurement

Frequency measurement almost invariably requires a counter and a reference clock oscillator. Here, the latter function is realized by a 4 MHz oscillator block controlled by an on-board quartz crystal. This device comes in an encapsulated metal enclosure with pins that fit into an IC socket. The output signal of the oscillator block is applied to a divider circuit composed of individual, cascaded counter ICs. The output pulses of the last counter are applied to a NOR gate, the second input of which is driven by the measured signal. The output signal of the NOR gate clocks a counter cascade for the duration of the gate time. When the gate time is over, the counter state — which is proportional to the frequency of the measured signal — is taken over by one of the PPI ports, which transfers it to the CPU. A small BASIC program translates the counter state into the corresponding frequency, which is shown on the monitor. Before the next measurement cycle, all counters are cleared by a reset pulse of accurately defined length, generated with the aid of a programmed port line and a monostable multivibrator.

Ports and peripherals

The 8255 is probably the best known programmable I/O device designed for use with Intel microprocessors. It provides 24 I/O pins which may be individually programmed in two groups of 12, and used in one of three modes of operation. The content of the control register on board the 8255 determines whether the port lines function as an input or an output. In Mode 0, each group of 12 I/O pins may be programmed in sets of four to be input or output. In Mode 1, each group may be programmed to have 8 lines of input or output. Of the remaining four pins, three are used for handshaking and interrupt control signals. The third mode of operation, Mode 2, is a bidirectional bus mode that uses 8 lines for a bidirectional bus, and 5 lines for handshaking, borrowing one from the other group.

The 8255 on the frequency meter card, IC$_1$, operates in Mode 0 with all port lines

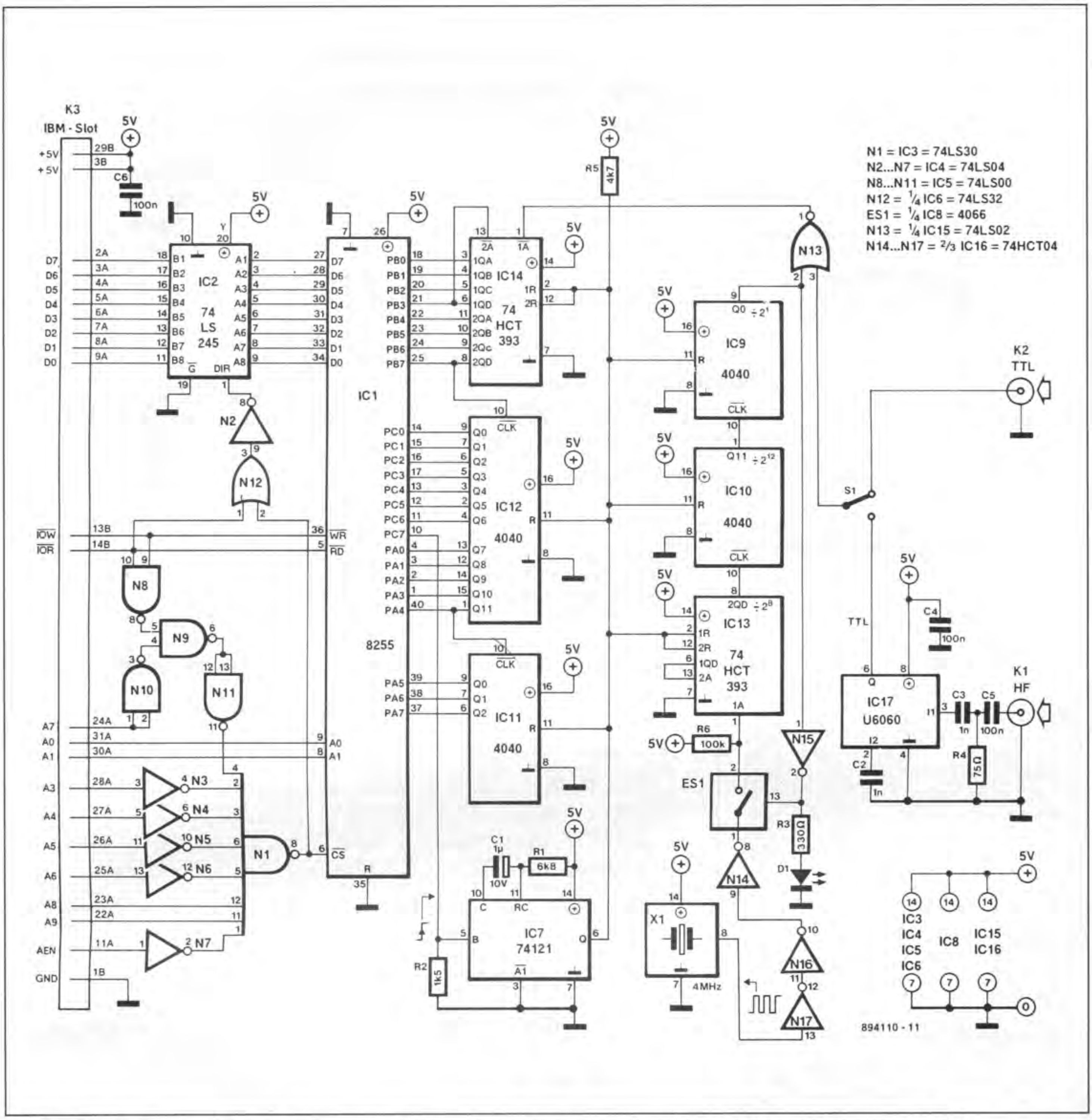


Fig. 1. Circuit diagram of the plug-in frequency meter card: the key components are the PPI, IC$_1$, and the prescaler, IC$_{17}$.

switched to inputs. Port C forms an exception, because one of its lines functions briefly as an output to supply the reset pulse for the counter cascade. The remaining pins of the 8255 are used to ensure correct interfacing with the CPU in the computer. PPI input pins $\overline{WR}$ (write) and $\overline{RD}$ (read) are driven direct by the PC expansion bus IOW (input/output write) and IOR (input/output read) signals that control the data direction. The 8255 is enabled by a low level at its $\overline{CS}$ (chip select) input. The $\overline{CS}$ signal is supplied by address decoder N$_1$.

PPI inputs PORT SELECT 0 (A0) and PORT SELECT 1 (A1), together with inputs $\overline{RD}$ and $\overline{WR}$, control the selection of the ports and the control register in the 8255.

Circuit details

The input of counter cascade IC$_{13}$-IC$_{10}$-IC$_9$ is clocked by 4 MHz crystal oscillator block X$_1$. The counters are reset at power-on, so that output Q0 of IC$_9$ is low. This level is inverted by N$_{15}$, and electronic switch ES$_1$ is consequently closed. The clock pulses are counted by IC$_{13}$, a Type 74HCT393 set to a divisor of 2^8. Its output pulses clock IC$_{10}$, which is configured to divide by 2^{12}. Counter IC$_9$, finally, provides a divisor of 2^1, and supplies an output signal with a period of about 0.524 s at pin Q0. Pin 2 of gate N$_{13}$ is held low until counter state $2^8 \times 2^{12} \times 2^1$ is reached. The measured signal taken from connector K$_2$ or the prescaler (IC$_{17}$) is applied to the second counter cascade, IC$_{14}$-IC$_{12}$-IC$_{11}$, via gate N$_{13}$. When the gate time (0.262 s) has lapsed, pin 2 of N$_{13}$ goes high. This results in ES$_1$ being opened, so that the measured signal is no longer processed.

Next, the CPU reads the dataword (bit-combination) provided by ports A, B and C of the PPI at adresses 300$_H$, 301$_H$ and 302$_H$ (768, 769 and 770 decimal). The counter state of IC$_{11}$, IC$_{12}$ and IC$_{14}$ is taken over as a 23-bit word for further processing. A series of BASIC commands (from line 910 onwards in the control program)

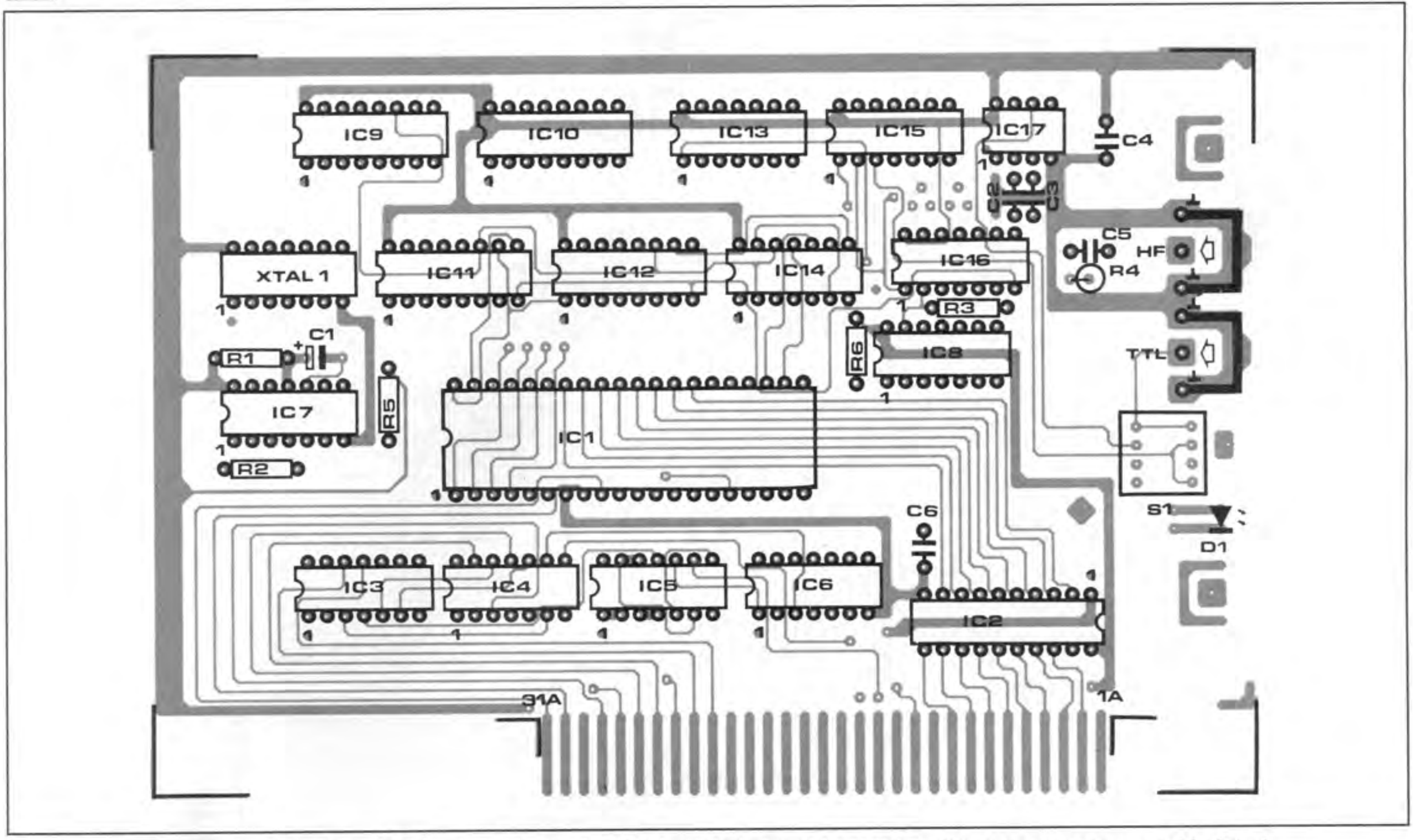


Fig. 2. **Component overlay of the double-sided, through-plated printed circuit board. The PC slot contacts are gold-plated.**

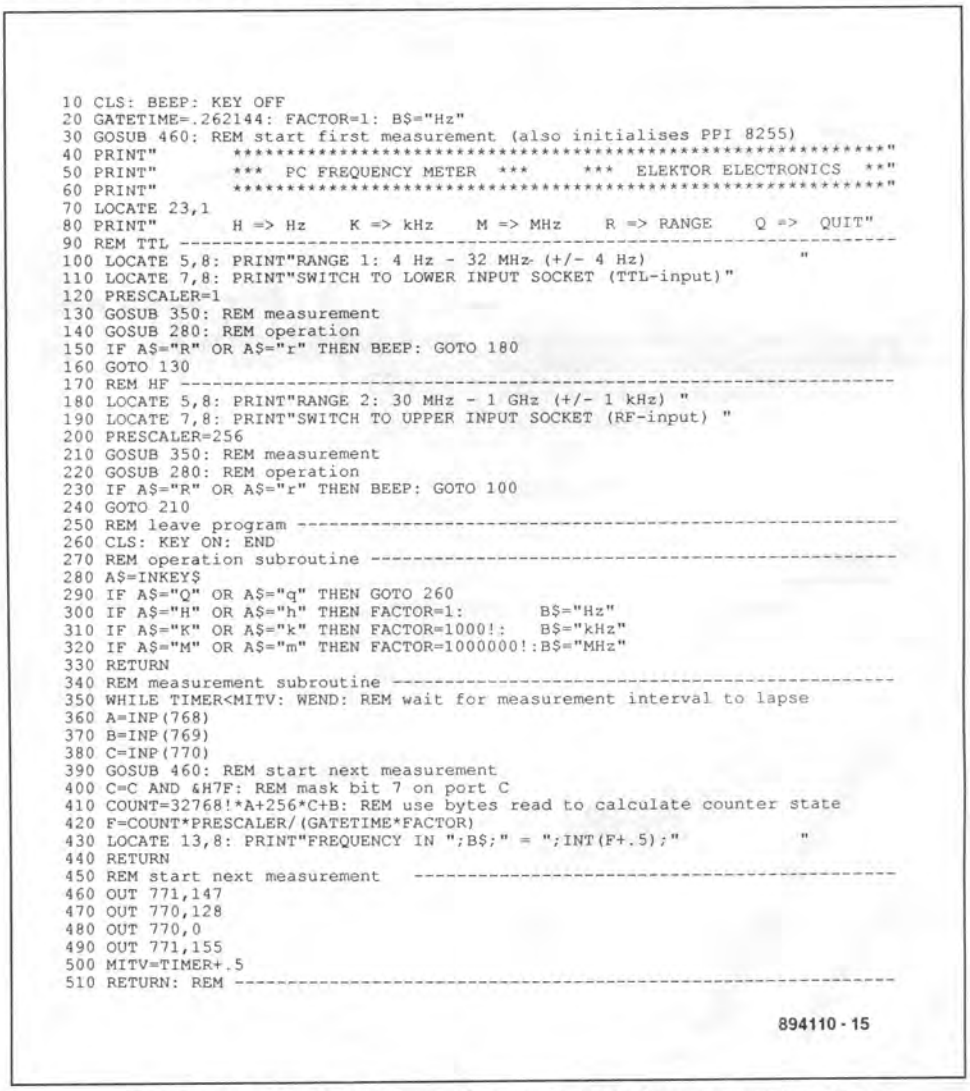
Parts list

Resistors:
R_1 = 6k8
R_2 = 1k5
R_3 = 330Ω
R_4 = 75Ω
R_5 = 4k7
R_6 = 100k

Capacitors:
C_1 = 1µ0; 10 V; radial
C_2;C_3 = 1n0
C_4;C_5;C_6 = 100n

Semiconductors:
D_1 = LED (5 mm)
IC_1 = 82555AC-2
IC_2 = 74LS245
IC_3 = 74LS30
IC_4 = 74LS04
IC_5 = 74LS00
IC_6 = 74LS32
IC_7 = 74121
IC_8 = 4066
IC_9;IC_{10};IC_{11};IC_{12} = 4040
IC_{13};IC_{14} = 74HCT393
IC_{15} = 74LS02
IC_{16} = 74HCT04
IC_{17} = U6060B (Telefunken)

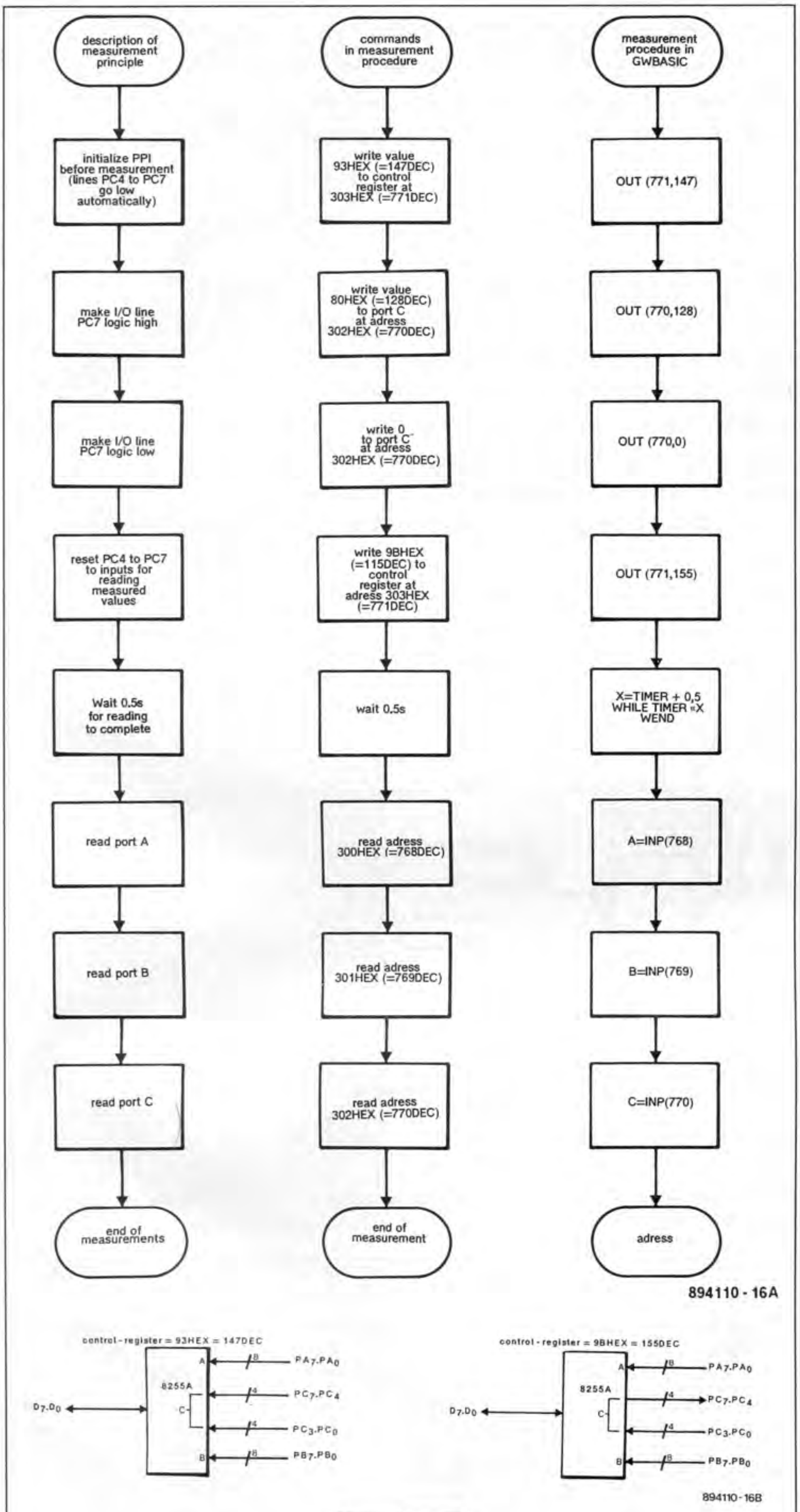
Miscellaneous:
S_1 = miniature SPDT switch for PCB mounting.
X_1 = 4 MHz oscillator block.
K_1;K_2 = RCA (phono) socket for PCB mounting.
PCB Type 894110 (see Readers Services page).



```
10 CLS: BEEP: KEY OFF
20 GATETIME=.262144: FACTOR=1: B$="Hz"
30 GOSUB 460: REM start first measurement (also initialises PPI 8255)
40 PRINT"         ************************************************************"
50 PRINT"         ***  PC FREQUENCY METER  ***      ***  ELEKTOR ELECTRONICS  **"
60 PRINT"         ************************************************************"
70 LOCATE 23,1
80 PRINT"        H => Hz     K => kHz     M => MHz     R => RANGE     Q =>  QUIT"
90 REM TTL ---------------------------------------------------------------------
100 LOCATE 5,8: PRINT"RANGE 1: 4 Hz - 32 MHz (+/- 4 Hz)                     "
110 LOCATE 7,8: PRINT"SWITCH TO LOWER INPUT SOCKET (TTL-input)"
120 PRESCALER=1
130 GOSUB 350: REM measurement
140 GOSUB 280: REM operation
150 IF A$="R" OR A$="r" THEN BEEP: GOTO 180
160 GOTO 130
170 REM HF ---------------------------------------------------------------------
180 LOCATE 5,8: PRINT"RANGE 2: 30 MHz - 1 GHz (+/- 1 kHz) "
190 LOCATE 7,8: PRINT"SWITCH TO UPPER INPUT SOCKET (RF-input) "
200 PRESCALER=256
210 GOSUB 350: REM measurement
220 GOSUB 280: REM operation
230 IF A$="R" OR A$="r" THEN BEEP: GOTO 100
240 GOTO 210
250 REM leave program ----------------------------------------------------------
260 CLS: KEY ON: END
270 REM operation subroutine ---------------------------------------------------
280 A$=INKEY$
290 IF A$="Q" OR A$="q" THEN GOTO 260
300 IF A$="H" OR A$="h" THEN FACTOR=1:       B$="Hz"
310 IF A$="K" OR A$="k" THEN FACTOR=1000!:   B$="kHz"
320 IF A$="M" OR A$="m" THEN FACTOR=1000000!:B$="MHz"
330 RETURN
340 REM measurement subroutine -------------------------------------------------
350 WHILE TIMER<MITV: WEND: REM wait for measurement interval to lapse
360 A=INP(768)
370 B=INP(769)
380 C=INP(770)
390 GOSUB 460: REM start next measurement
400 C=C AND &H7F: REM mask bit 7 on port C
410 COUNT=32768!*A+256*C+B: REM use bytes read to calculate counter state
420 F=COUNT*PRESCALER/(GATETIME*FACTOR)
430 LOCATE 13,8: PRINT"FREQUENCY IN ";B$;" = ";INT(F+.5);"               "
440 RETURN
450 REM start next measurement   ----------------------------------------------
460 OUT 771,147
470 OUT 770,128
480 OUT 770,0
490 OUT 771,155
500 MITV=TIMER+.5
510 RETURN: REM ----------------------------------------------------------------
```

894110 - 15

Fig. 3. **Listing of the GWBASIC program that controls the frequency meter card.**


description of measurement principle
initialize PPI before measurement (lines PC4 to PC7 go low automatically)
make I/O line PC7 logic high
make I/O line PC7 logic low
reset PC4 to PC7 to inputs for reading measured values
Wait 0.5s for reading to complete
read port A
read port B
read port C
end of measurements
commands in measurement procedure
write value 93HEX (=147DEC) to control register at 303HEX (=771DEC)
write value 80HEX (=128DEC) to port C at adress 302HEX (=770DEC)
write 0 to port C at adress 302HEX (=770DEC)
write 9BHEX (=115DEC) to control register at adress 303HEX (=771DEC)
wait 0.5s
read adress 300HEX (=768DEC)
read adress 301HEX (=769DEC)
read adress 302HEX (=770DEC)
end of measurement
measurement procedure in GWBASIC
OUT (771,147)
OUT (770,128)
OUT (770,0)
OUT (771,155)
X=TIMER + 0,5 WHILE TIMER <X WEND
A=INP(768)
B=INP(769)
C=INP(770)
adress
894110 - 16A
control - register = 93HEX = 147DEC
control - register = 9BHEX = 155DEC
8255A
A
B
C
D7-D0
PA7-PA0
PC7-PC4
PC3-PC0
PB7-PB0
8
4
894110 - 16B

address		register
dec	hex	
768	300	port A
769	301	port B
770	302	port C
771	303	port D

Fig. 4. Flow-charts of the control program, and functional representation of the PPI in the address space it occupies in the PC.

then takes effect. Port C is briefly switched to output and supplies dataword FF_H (255 decimal). The leading edge of the signal at pin PC7 triggers monostable multivibrator IC_7, which responds by resetting all counters by means of its output signal at pin 6. A counter state of 0 results in a low level at the input of N_{15}. Also, ES_1 is closed, so that the circuit is ready for a new measurement cycle.

The fact that the CPU starts every measurement cycle by making PC7 high already indicates that it has ample time to read the port contents, calculate the frequency, and update the screen. Moreover, the clock oscillator is automatically disabled after the gate time. Not surprisingly, therefore, the speed offered by BASIC is ample for the control program.

The 1 GHz prescaler, IC_{17}, is a Type U6060 from Telefunken, originally designed for use in PLL-controlled TV tuners. The chip has a balanced input (which is not used here), a fixed divide-by-256 prescaler, and a TTL output level converter. The input sensitivity of the 50 Ω input is better than 20 mV for frequencies between 30 MHz and 1,000 MHz.

Addresses

An address decoder set up around IC_3, IC_4 and IC_5 monitors the logic levels on expansion bus address lines A3 through A9. The $\overline{CS}$ input of the 8255 is actuated only when A3 through A6 are low, and A8 and A9 are high, in combination with the AEN (address enable) line. When the 8255 is enabled, one of its four registers is selected by the bit combinations on A0 and A1. This means that the frequency meter card occupies the four I/O addresses, 300_H through 303_H, provided for prototyping cards in the PC. If any other extension card in the PC occupies the same addresses, it must be relocated by altering its jumper configuration as specified by the manufacturer. In general, extension cards can not share I/O address space without causing bus contention problems.

Software

The operation of the BASIC control program for the frequency meter may be analyzed in three ways as shown by the respective flow diagrams in Fig. 4. The BASIC program itself (Fig. 3) is straightforward, offering a kind of minimum user interface. The program is simply typed in under GWBASIC (available on any MS/DOS PC), saved to disk, and started with the RUN command. LED D_1 flashes during measurements to indicate activity of the card. The program prompts you to select between the LF/TTL input and the HF input, and automatically switches between kHz and MHz readings on the screen.

INTRODUCTION TO DUOBINARY ENCODING AND DECODING

J. Buiting

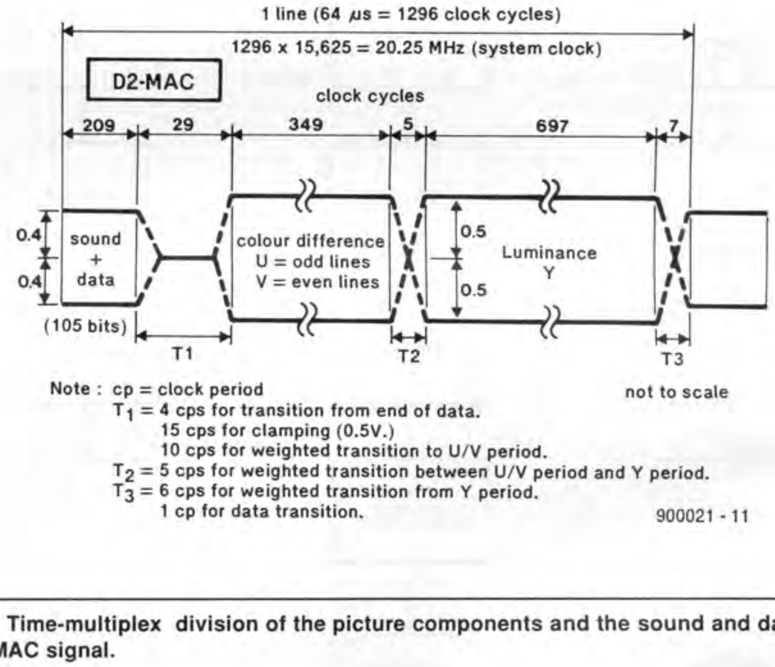
With a dozen or so MAC TV signals available from satellites such as TV-SAT2, TDF-1, Olympus, Astra and, shortly, BSB, it is surprising to note that relatively few electronics engineers and satellite-TV reception enthusiasts appear to be aware of essential technical backgrounds to MAC. In line with the theme of the month, communications, this article looks at one aspect of the MAC transmission standard that has received little attention so far: duobinary encoding and decoding of the sound and data block.

Several new TV transmission standards were studied and discussed following the channel and orbital position assignments drawn up by WARC 77. Although these studies resulted in proposals for different systems, all and sundry agreed on the need of analogue picture transmission and digital sound transmission on the basis of a time-multiplex scheme instead of a frequency-multiplex scheme as used up to then for the PAL, SECAM and NTSC systems for existing terrestrial TV broadcasts.

The proposals for A-MAC and B-MAC systems were short-lived because they did not provide a complete separation of the picture and sound blocks at the modulation signal level, and in addition were hard to implement in existing satellite TV channel bandwidths (note, however, that B-MAC is still used in Australia). A third standard, C-MAC, developed by the IBA and accepted as well as recommended by the EBU, uses a time-multiplex modulation signal in which the frequency-modulated analogue picture components are interspersed with a 2-4 PSK modulated sound and data block with a data rate of 20.25 Mbit/s. This makes C-MAC suitable for transmission by existing communications service satellites such as the ones in the Intelsat and Eutelsat series, but not for direct-to-home transmission and distribution in TV cable networks.

D-MAC/Packet and D2-MAC Packet

The need of feeding MAC signals into existing TV cable networks with limited



Note : cp = clock period
T_1 = 4 cps for transition from end of data.
15 cps for clamping (0.5V.)
10 cps for weighted transition to U/V period.
T_2 = 5 cps for weighted transition between U/V period and Y period.
T_3 = 6 cps for weighted transition from Y period.
1 cp for data transition.

Fig. 1. **Time-multiplex division of the picture components and the sound and data block in a D2-MAC signal.**

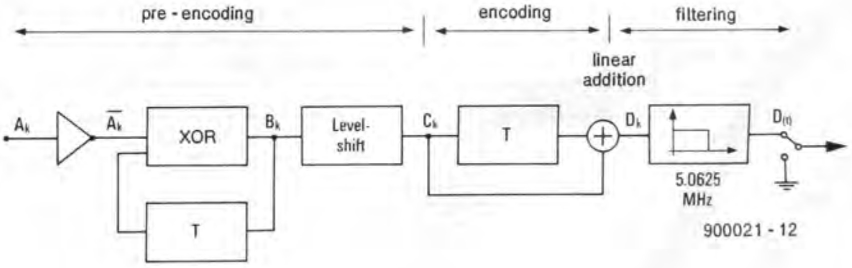


Fig. 2. **Basic structure of a duobinary encoder. The two blocks marked 'T' are one-bit time delays (*illustration courtesy Blaupunkt GmbH*).**

Sound encoding for D2-MAC/Packet

Sampling rate	1. 32 KHz (HQ) stereo and mono at high quality (40–15,000 Hz) 2. 16 kHz (MQ) Mono at medium quality (40–7,000 Hz)
Quantization	14-bit
Data form	2's complement
Coding	1. Linear, 14-bit (L) 2. NICAM, 10-bit (I)
Error correction	1. Parity check (1) 2. Hamming code (2)
Sound transmission options	1. Parity check for 6 MSB at 10-bit NICAM Capacity: e.g., HQI1 with 4 mono channels 2. Parity check for 11 MSB at 14-bit Linear Capacity: e.g., HQL1 with 3 HiFi mono channels 3. (11,6)Hamming for 6 MSB at 10-bit NICAM Capacity: e.g., HQI2 with 3 HiFi mono channels 4. (16,11)Hamming for 11 MSB at 14-bit Linear Capacity: e.g., HQL2 with 2 HiFi mono channels
Scale factor	covers 32 samples for options 1, 2 and 3 (1 ms at 32 kHz) covers 18 samples for option 4 (562.5 µs at 32 kHz)

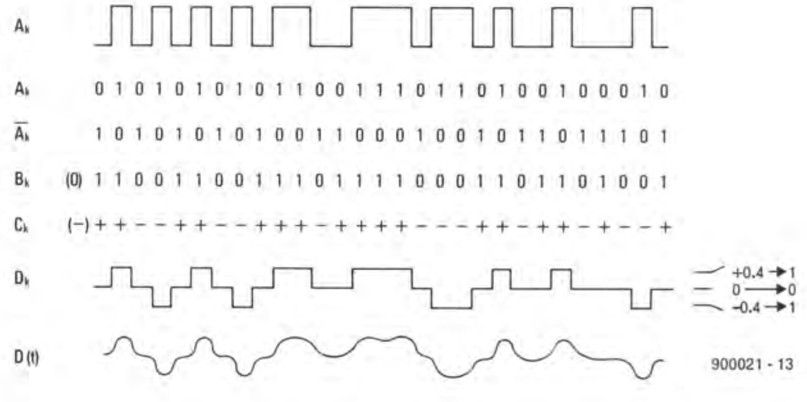


Fig. 3. Pulse levels and waveforms at various stages of the duobinary encoding process.

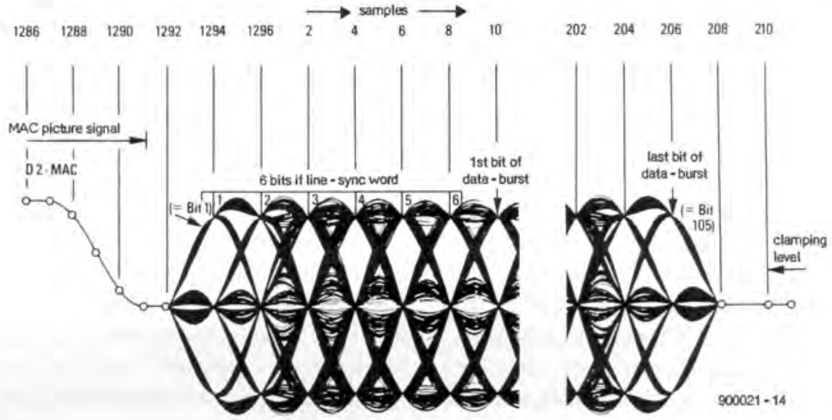


Fig. 4. Waveform of the three-level signal that forms the data/sound burst in a time-multiplexed MAC picture line. (*illustration courtesy Blaupunkt GmbH*)

channel bandwidth prompted workers at several radio and television laboratories to look for a means of reducing the bandwidth of C-MAC from about 22 MHz to a value lower than about 10 MHz. The proposals of the CCETT laboratories at Rennes, France, form the basis of the D-MAC/Packet system. This fatures duobinary encoding of the sound and data block (Packet), so that it can be frequency-modulated like the picture signals, obviating a switch-over at RF level to 2-4 PSK as with C-MAC. The data rate, however, is the same: 20.25 MHz. The D-MAC/Packet system is to be used for all BSB channels to be taken into operation shortly. It offers eight high-quality sound channels, and requires a channel bandwidth of about 10.5 MHz.

The D2-MAC system accepted by most continental European countries is a further development of the D-MAC system. The figure '2' in D2-MAC indicates the bit rate reduction factor with respect to D-MAC. The sampling clock frequency of 20.25 MHz is the same as with C-MAC and D-MAC, but the data bit rate is reduced to 10.125 MHz, so that every second sampling pulse reads one bit. The resultant bandwidth reduction from 10.5 MHz to about 7.8 MHz is sufficient to enable the extensive cable-TV networks on the European continent to carry D2-MAC signals in VSB AM channels. The D2-MAC system supports eight medium-quality or four high-quality sound channels. Both D2-MAC and D-MAC allow NICAM-728 signals to be transmitted. Extensive studies are currently being made into the conversion of both systems into a version that allows HDTV pictures to be transmitted.

Duobinary encoding

The content and digital structure of the sound and data signals are not discussed here, i.e., no consideration will be given to the separation of sound and data, error correction, NICAM-728, compression techniques, quantization factors and the like. The focus of the discussion below is on how the digital data that forms the sound and data to accompany the MAC picture is treated to achieve the bandwidth reduction required for cable-TV systems and direct-to-home reception.

The position of the sound and data block in the time-multiplexed modulation signal fed to the uplink transmitter is shown in Fig. 1. Note that the amplitude is 0.8 Vpp as compared to 1 Vpp for the multiplexed analogue picture components (colour difference and luminance). For D-MAC/Packet, the sound and data block consists of 209 bits instead of 105 as shown for the D2-MAC/Packet system.

The operations involved in duobinary encoding are shown schematically in Fig. 2. The digital datastream A_k is pre-coded to give a datastream Bk. A_k is first inverted, and subsequently combined with the 1-bit delayed (T) result of a XOR operation. In Boolean notation:

$$B_k = Ak \oplus B_{k-1}$$

Next, the 0s and 1s in the datastream B_k are level-shifted to give −1 and +1 levels in the datastream C_k:

$$C_k = 2\,B_k - 1$$

Pre-coding is used to restrain the otherwise unlimited error propagation.

The pre-coded signal is subjected to a delay, T, linearly added to itself, and amplitude-limited to give datastream D_k.

$$D_k = (M/4)(C_k + C_{k-1})$$

Where M equals 80% of the maximum video amplitude. Amplitude limiting at a fixed factor is required to prevent the duobinary encoded signal exceeding the maximum level of the picture signal.

The datastream D_k can have three instantaneous levels: +0.4 V, −0.4 V and 0 V. The first two represent a logic 1, the last one a logic 0.

The timing diagram in Fig. 2 shows a practical example of how the previously discussed steps convert the digital datastream, A_k, into a duobinary datastream, D_k. The reduced bandwidth requirement of D_k is immediately apparent by looking at the duobinary signal that results from the five 0-to-1 transitions at the start of A_k. Subsequent 1s in A_k cause no level change in D_k, which remains at +0.4 V or −0.4 V (remember that the amplitude of D_k in the modulation signal is 0.8 Vpp). For an odd number of 0s in between two 1s, D_k changes from 0.4 V via 0 V to −0.4 V or the other way around. For an even number of 0s, the signal reverts to the previous level.

Referring back to Fig. 1, D_k is passed through a low-pass filter to reduce the bandwidth requirement of the 10.125 Mbit/s (D2-MAC) databurst to about 5 MHz. The addition of the picture components and frequency modulation of the resultant time-multiplexed signal gives rise to a bandwidth of between 7 MHz and 8 MHz (D2-MAC), which is suitable for cable-TV networks.

The filtered three-level component in the modulation signal is illustrated in Fig. 3. Note that the sound and data block is located between the end of the luminance component and the start of the clamping level reference period. The block starts with the 6-bit line synchronization word, LSW, which is either true (LSW) or inverted ($\overline{\text{LSW}}$) to indicate whether the line belongs with the odd- or the even-numbered raster in the interlaced picture.

Abbreviations used in this article

AM = Amplitude Modulation
BER = Bit Error Rate
BSB = British Satellite Broadcasting
CCETT = Centre Commun des Etudes Téléphonie et Télévision
EBU = European Broadcasting Union
HDTV = High Definition Television
MAC = Multiplexed Analogue Components
PAL = Phase Alternation Line
PSK = Phase Shift Keying
SECAM = Séquentiel Couleur à Memoire
VSB = Vestigial Side Band
WARC = World Administrative Radio Conference
XOR = Exclusive OR

At the receiver side: duobinary decoding

The baseband output signal of a satellite-TV receiver tuned to a MAC transmission contains the duobinary encoded signal $D_{(t)}$ received from the TV satellite. Two comparators with adjustable slicing levels may be used as shown in Fig. 4 to recover the original datastream A_k which contains the sound and data bits. In practice, the data-slicer is integrated into a MAC decoder chip such as the DMA2280 from ITT Semiconductors. To achieve a low BER, the DMA2280 allows the upper and lower slicing levels to be adjusted with the aid of an internal register.

Conclusions

Duobinary encoding and decoding are relatively simple operations that result in a significant bandwidth reduction of MAC signals transmitted by high- and medium power TV satellites. Experiments have shown that the system is highly immune to reflections and phase delays typically introduced in large cable systems.

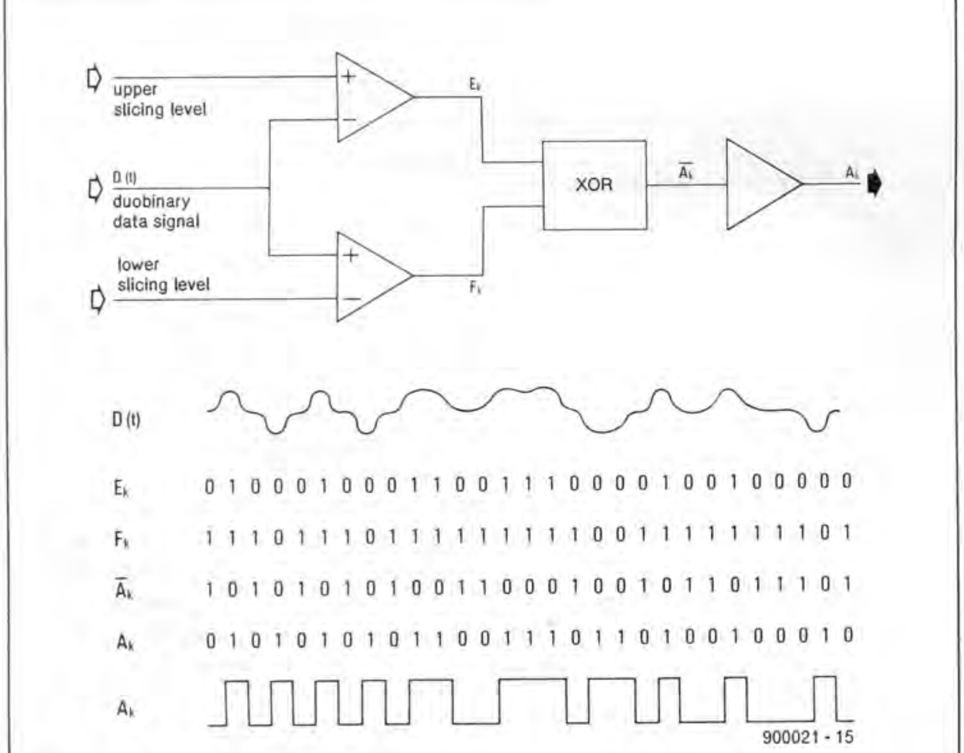

upper
slicing level
D (t)
duobinary
data signal
lower
slicing level
+
−
+
−
Eₖ
Fₖ
XOR
Āₖ
Aₖ
D (t)
Eₖ 0 1 0 0 0 1 0 0 0 1 1 0 0 1 1 1 0 0 0 0 1 0 0 1 0 0 0 0 0
Fₖ 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 0 1
Āₖ 1 0 1 0 1 0 1 0 1 0 0 1 1 0 0 0 1 0 0 1 0 1 1 0 1 1 1 0 1
Aₖ 0 1 0 1 0 1 0 1 0 1 1 0 0 1 1 1 0 1 1 0 1 0 0 1 0 0 0 1 0
Aₖ
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Fig. 5. Basic operation of a duobinary decoder that recovers the original sound and data bitstream marked A_k (*illustration courtesy Blaupunkt GmbH*).

SCIENCE & TECHNOLOGY

CONVERSING WITH COMPUTERS – NATURALLY

by Professor Marcel Tatham, Department of Language and Linguistics, University of Essex

For the past 20 years or so, a great deal of research has been aimed at enabling users of computers to communicate with their machines by voice only, instead of by keyboards and visual display units. What at first appeared to be relatively easy, getting a computer to talk with a human-like voice and making it able to respond appropriately when spoken to, has turned out to be extremely difficult. It is so difficult that we can now confidently predict that it will be several decades before fully natural, free-flowing conversation can take place between people and machines. Only now are we beginning to develop systems that perform the task in an acceptable way, though in certain restricted areas conversation with computers is already with us.

The scenario of a conversational system with a machine requires us to picture using a computer to replace one of a pair of human beings speaking to one another, that is, using the machine to simulate the behaviour involved in carrying out one side of the conversation. So we can begin by examining in general terms what it is that a person does during the communication process.

On the surface, what happens looks simple enough: when someone is spoken to, the immediate response is to speak back, enabling information to flow back and forth between the two speakers. We can model this behaviour as consisting of three separate components:

(1) hearing the message or question;
(2) thinking about how to respond;
(3) speaking the response.

Hearing is in fact a two-stage process. The speech signal enters the ear and almost immediately a complex acoustic analysis takes place in the inner ear. This is a passive process involving no thought on the part of the listener. The results of the analysis are sent to the brain where, in a second stage, cognitive processing takes place to further refine the analysis and to 'label' the data as particular speech sounds or words.

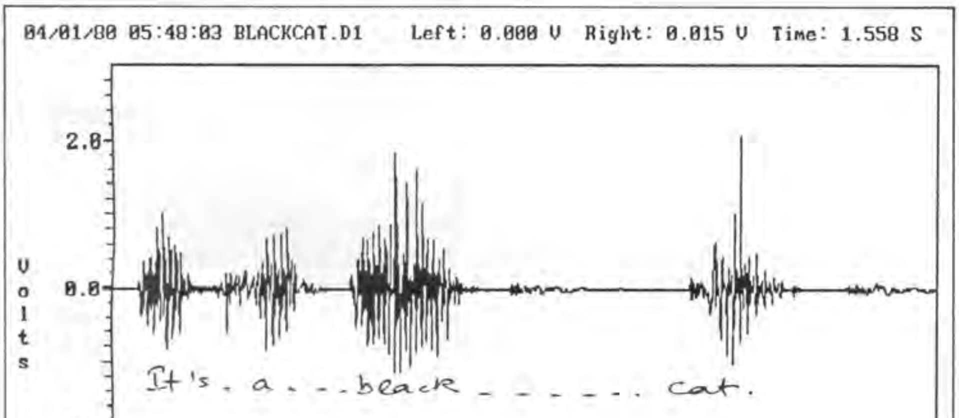


Fig. 1. Acoustic signal of the sentence "it's a black cat." It is easy to spot the individual words.

Before any response to the perceived signal can be generated, cognitive processes must take place that result in the listener's understanding of what has just been heard. Only when the message has been understood can the listener compose a suitable response.

Two stages are involved in speaking the response. First, the message needs to be encoded linguistically: thought is turned into language as preparations are made to adjust the speech organs to produce the appropriate acoustic signal. Second, a quite complex process of neuromuscular control is brought into play to make sure that lungs, vocal cords, tongue, lips and so forth are organized to produce the right sounds at the right time.

The processes are repeated over and over by each participant in the conversation as the exchange of information unrolls.

Simulating conversation

The basic idea of replacing one human being by a machine is simple enough: programs replace in turn the three stages of the human process being simulated. The first stage is parallel to the hearing process. A microphone picks up the speech signal and a program simulates the ear's analysis of the acoustic signal. The results of this analysis are processed by a second program which conducts the labelling task: the acoustic signal is identified as containing particular speech sounds that in combination represent individual words.

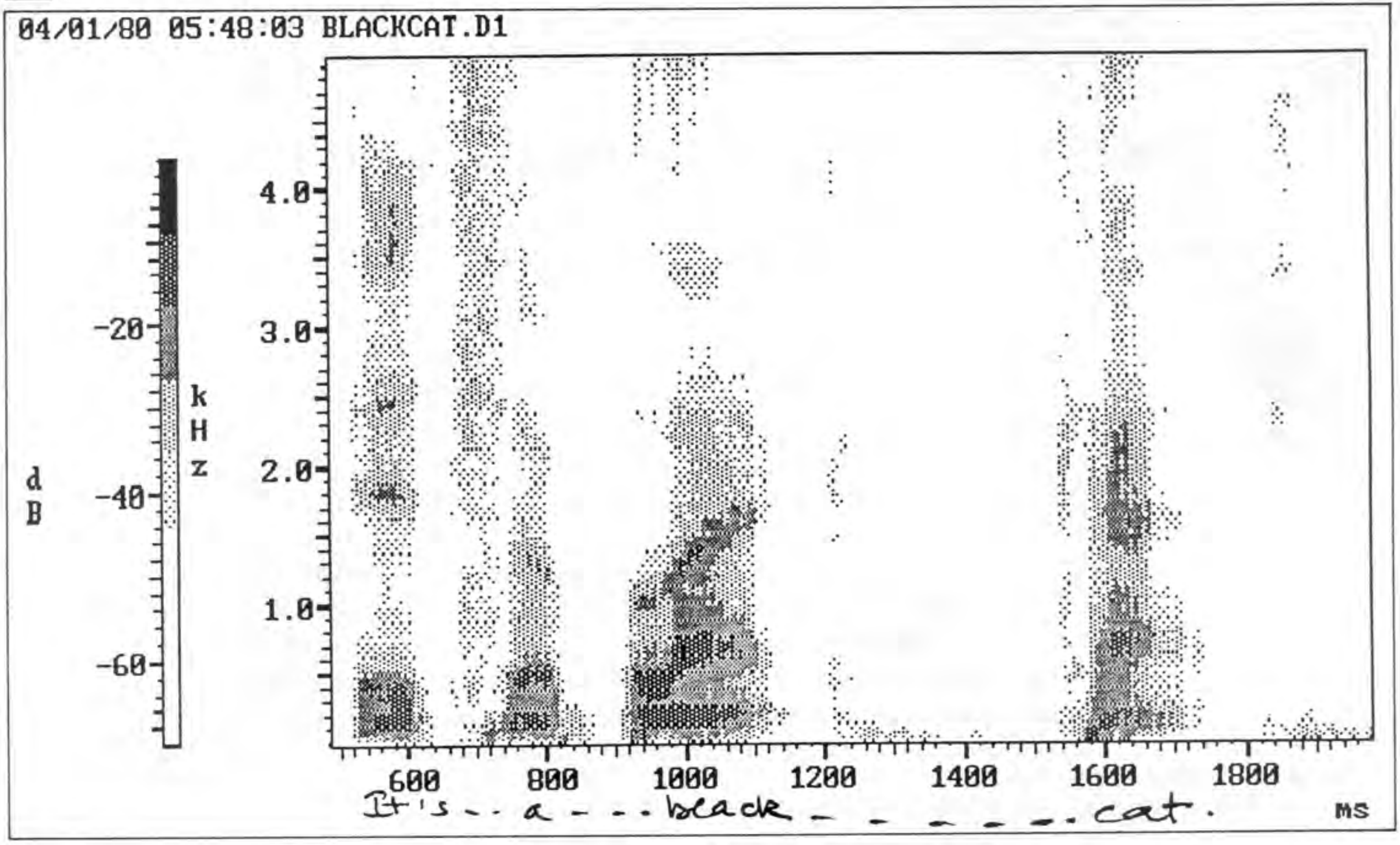


Fig. 2. Acoustic analysis by computers of the sentence in Fig. 1. In this, a kind of map of the inner details of the signal, the boundaries between the words are still easily detected.

The stage is usually called 'automatic speech recognition'.

The next stage in the simulation is to copy the human process of understanding the message content of the speech just received. We call this 'speech understanding', and it is by far the most difficult part of the system in which to achieve satisfactory results. People understand speech in the context of their accumulated experience of the world. Obviously, to put such knowledge into a computer is a vast, if not impossible, task. In practice ways are found of getting around the problem, usually by restricting the area of conversation as much as possible, so that the contexts the computer must know to interpret the information are narrowed down to a manageable size. The processes involved are studied within the field of artificial intelligence, which here means simulating the cognitive behaviour of people.

Once the computer has understood what has been said to it, it is able to formulate a response which must then be spoken. Speech synthesis forms the final stage of the process. A program takes the linguistically encoded response and, mimicking the way a human being produces an acoustic signal, produces speech through a loudspeaker.

Experience and labelling

The most difficult part of getting computers to hold conversations with people is the simulation of the cognitive processing involved in understanding what the person has said and in formulating an appropriate response. The reason for this is that speech signals do not contain within themselves all the information needed for their understanding. Take the simple sentence "it's warm today." Spoken during the winter this might mean that the temperature has risen to 10 degrees, but spoken at the height of summer it might well mean that the temperature has reached 25 degrees. Human beings talking to one another know whether it is winter or summer; the computer does not. All of us have spent our lifetimes acquiring such information which we use every time we interpret what is said to us. The problem is how to give the computer just the right 'experience' to be able to put what it hears into context and reach an understanding of the message.

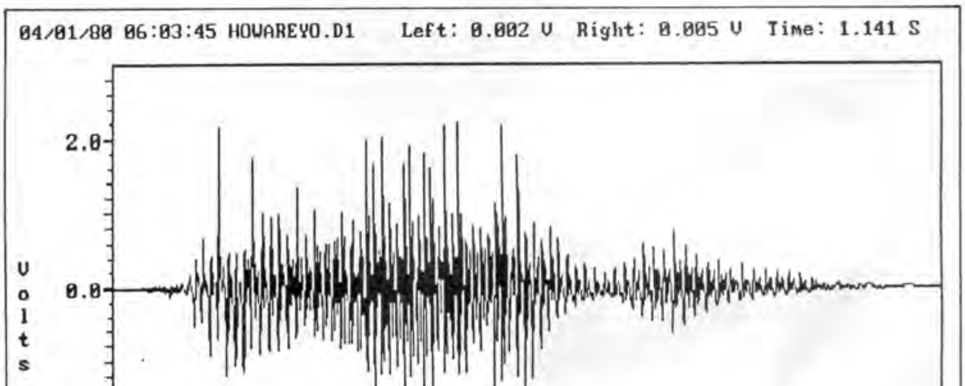


Fig. 3. Waveform of the sentence "How are you?" Because the consonants are spoken in much the same way as we speak vowels, the words are blurred together.

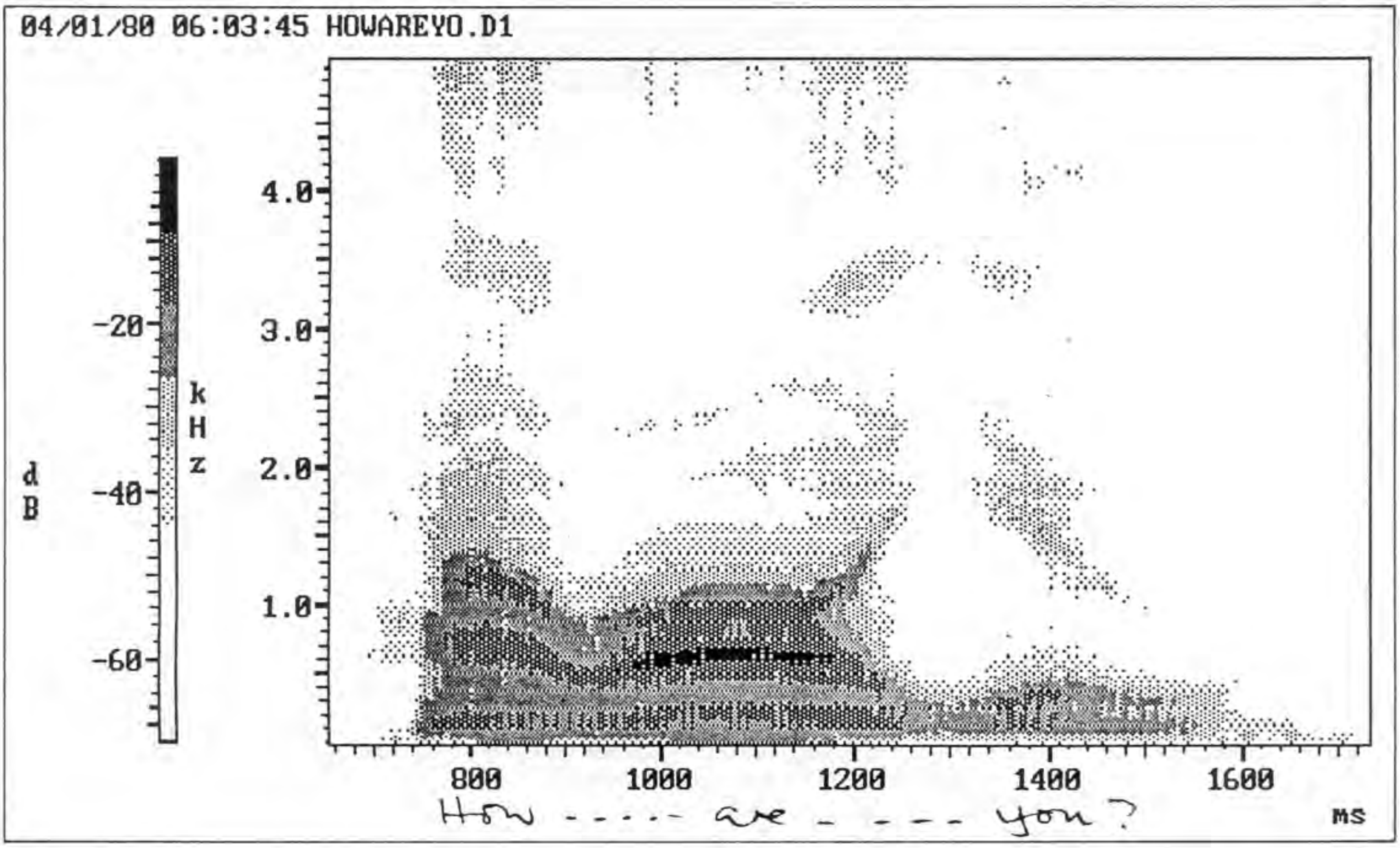


Fig. 4. Analysed version of the waveform in Fig. 3. For this phrase the segmentation of individual sounds and words is by no means obvious.

But even if we are able to limit the topic of conversation in such a way that the computer stands some chance of understanding what is said to it, there is also the difficult task of converting the sound it hears into the sentences it must understand. Figure 1 shows the acoustic signal of the spoken sentence "it's a black cat." In the waveform, time runs from left to right and it is easy to spot, by looking at the way in which the amplitude of the tracing changes, the individual words in the sentence. Labelling this signal is not at all difficult because it is naturally segmented. It consists of alternating consonants (without loud vocal cord vibration) and vowels (with loud vocal cord vibration). It is the alternation that results in the widening and narrowing of the trace. Figure 2 shows the acoustic analysis the computer performs on the same sentence, producing a kind of map of the inner details of the signal. Once again, the boundaries between the words are easily detected.

Sentences are rarely this easy to segment, however. In Fig. 3 we see the waveform of the sentence "How are you?" Although in the spelling of this sentence we see orthographic consonants and vowels alternating, the particular consonants here (w, r, y) are spoken in much the same way as we speak vowels. The result is a blurring together of the words, making it almost impossible to spot the boundaries between them. If we look at Fig. 4, which is the analysed version of the same sentence, we can see that the segmentation of the individual sounds and words that make up the phrase is by no means obvious.

Synthesizing the response

The easiest component of the system is the synthesis of the message the computer has generated in response to what it has heard. Assuming the problems of the earlier stages have been overcome and that the computer has formulated what it wants to say, the response must now be spoken. In some sense the task here is the opposite of the labelling one: the computer has generated the right labels and arranged the words to form a sentence, and now the acoustic signal has to be generated. The building blocks used to form the spoken sentence are individual sounds but, as we saw above, people do not speak sequences of isolated sounds. They run them together. Blurring the boundaries between speech segments forms the basis of good speech synthesis, and success depends on accurately generating the different types of blurring, as shown by Figures 1 and 3.

Conversations with computers will be a success only when everything is as natural as between two human beings. Each of the stages described above can now be accomplished with varying degrees of success, and we have complete systems in operation in the laboratory. But they are unnatural in that, for example, the computer cannot detect the subtleties hidden within human speech nor reproduce them when it speaks. These subtleties largely communicate peoples' attitudes, feelings or emotions. We can say the simple word "hello" in such a way that it communicates how pleased we are to see someone; or how relieved we are they have shown up; or how angry we are; or how surprised, and so on. Research is well under way to determine just how a person communicates such emotive subtleties in speech, and how these can be detected and reproduced by the computer. Preliminary results of incorporating this research into our conversational simulations show naturalness to be considerably improved.

It will be some time before holding what seems a quite natural conversation with a computer will be a common everyday occurrence. But already, computers that understand us and can respond by speaking back are beginning to make their appearance. In certain restricted areas, such as information services available over the telephone, experimental systems are already in use. Banking transactions and airline time-table services are the first of such systems becoming available, and as we improve the conversational abilities of the computer we shall see a rapid expansion of interaction between human beings and computers, not using keyboards and screens but natural-sounding speech.

LETTERS

CENTRONICS COMPATIBLE PRINTER BUFFER

Dear Sir — In your March 1989 issue, there is the Centronics-compatible printer buffer. Is this available ready-made or as a kit?
B. Hobart, Ontario, Canada.

As far as we know, the printer buffer is not available ready-made, but a kit is available from ***C-I Electronics, P O Box 22089, 6360 AB NUTH, the Netherlands.***

MIDI KEYBOARD CONTROLLER

Dear Sir — Could you please supply me with the names and addresses of the manufacturer and UK suppliers for the Type E510 MIDI keyboard controller chip (June 1989 issue).
R. Payman, St. Albans, Herts.

This chip is made specially for Doepfer Elektronik and is available only from ***C-I Electronics, P.O. Box 22089, 6360 AB NUTH, The Netherlands.***

DESIGNING BAROMETERS FROM SIMPLE CIRCUITRY

Dear Sir — I would appreciate the name and adress of the suppliers of the LT1014DN and SCX15ANCV devices used in the design of the barometers in your January 1989 issue.
E.J. Marchant, Tokoroa, New Zealand.

The SCX15ANC sensor is manufactured by Sensortechnics and is available in the UK from Sensortechnics UK, 30 Regent Place, RUGBY CV21 2PM, Telephone (0788) 80426.
The LT1014DN is produced by Linear Technology Corp. and is available in the UK from Dialogue Distribution, Wicat House, 403 London Road, CAMBERLEY GU15 3HL, Telephone (0276) 682001.

AN 80 W HI-FI LOUDSPEAKER SYSTEM

Dear Sir — Regarding "Triplet: an 80 W hi-fi loudspeaker system", are there any distributors of SEAS speakers in Canada?
L.F. Barsoney, Ottawa, Canada.

The SEAS distributors for Canada are: SOLEN, 4470 Thibault Ave, St. Hubert, QC J3Y 7T9, Telephone (514) 656-2759.

POWER INVERTERS

Dear Sir — I kindly ask you to inform me if you have published any books about single or three-phase sinus inverters.
C. Goncalves, Oporto, Portugal.

We have not, but your requirements may be met by Power Electronic Converters, *a series of four volumes published by North Oxford Academic Publishers, London. Another work that looks suitable is* Power Electronics (ISBN 0 13 686619) *published by Prentice Hall, Hemel Hempstead, England.*

THE WAY AHEAD

Dear Sir — As a long-time reader and builder of many of your projects, I must ask you what direction your magazine is taking. Over the past eighteen months or so, you have published articles on computers and controllers with dedicated processors and also boards using surface mount components.

Some of the processors featured, such as the 8751 and 8748 can not be modified without very expensive programmers, well out of the reach of most hobbyists.

Surface-mount components are still hard to obtain and, without specialist equipment, fairly difficult to fit.

Has the hobbyist still a hope of modifying or adapting designs to his own requirements or must he face a future in which he can only buy specialist kits for which he needs a fair amount of expensive test equipment?
G. Clements, Harrow, Middlesex.

We have received a number of letters from readers in similar vein. The aim of Elektor Electronics *is to cater for a broad readership: from experienced amateurs through students of electrical/electronic engineering to professional technicians and engineers. We think that a large majority of our readers are very enthusiastic people who are interested in virtually all aspects of electronics: from audio and hi-fi through computers, information technology and robotics to radio, TV and satellite communications. Many of them, we feel, are also curious about the frontiers of technology whence, for instance, our Science & Technology column and other articles on advanced electronics.*

Many of the projects we publish are designed in our own international laboratories, but quite a number come from freelance contributors from all over the world. Although our designers are trained in electrical/electronic engineering, not all of them are fully qualified engineers. All of them, however, are enthusiastic experimentalists aware of most of the needs and interests of both professional and amateur electronic designers.

It is true that although in the professional world surface mount technology has not only won the battle but is also winning the war, it is still an area fraught with difficulties for most amateurs (and not a few professionals!). None the less, as publishers of a serious publication, we must deal with, and make our readers conversant with, the technique.

Similarly, there is no stopping new types of processor entering every aspect of electronics and most readers, we feel, want to be acquainted with them, even if they can not (as yet) afford to buy them. Also, such devices have a habit of becoming less expensive quite quickly. At the same time, we still publish projects that use such old faithfuls as the nearly 20-year old 555!

We continuously have to judge where the dividing line between the impossible and the interesting and affordable lies – and no doubt we sometimes misjudge. Nevertheless, we are determined to continue to strive to give all our readers something to look forward to in every one of our issues: from the relatively simple – witness the series of Intermediate Projects *introduced early last year – to the difficult, such as the* Centronics-compatible printer buffer *(Sept. 1989) or the* ATN Filmnet Decoder *(March 1989).*

SURFACE ACOUSTIC WAVE DEVICES

Dear Sir — I wonder if you could let me have the name and address of manufacturers or suppliers of surface acoustic wave devices for radio remote control.
P. Elphick, Edinburgh.

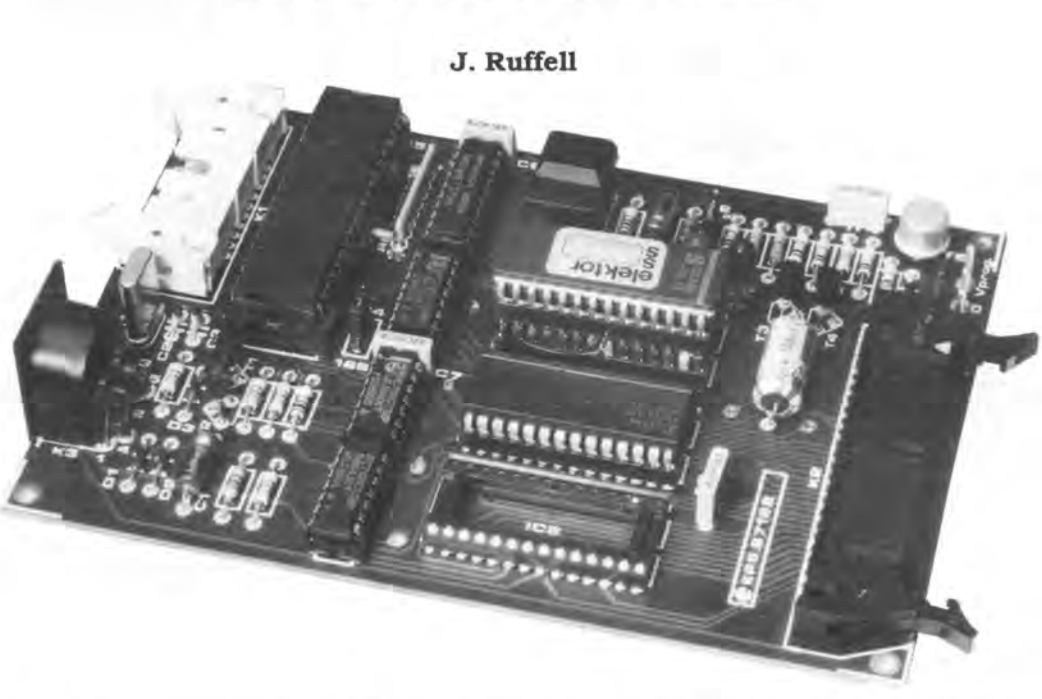
Information on SAWs may be obtained from Siemens Ltd, Siemens House, Windmill Road, Sunbury-on-Thames TW16 8HS, Telephone (09327) 85691. Many Siemens devices are available from ElectroValue Ltd, 28 St. Judes Road, Englefield Green, EGHAM TW20 0BH, Telephone (0784) 33603.

ELECTRONIC DESIGNS FOR POSSIBLE MANUFACTURE

In response to letters from a number of readers on how to place electronic designs with manufacturing companies, we must advise that we have no entree with any manufacturing companies. We suggest that these readers seek the advice from the **British Radio & Electronic Equipment Manufacturers' Association, Landseer House, 19 Charing Cross Road, LONDON WC2H 0ES, Telephone 01-930 3206.**

CMOS REPLACEMENT FOR 8052AH-BASIC

J. Ruffell



Simple to program and implement for a wide range of applications requiring intelligent control, the BASIC computer described roughly two years ago is now due for a modification that reduces its current consumption by a factor of four. A small BASIC program written for the occasion, a terminal or PC running a terminal emulation program, an Intel-hex compatible EPROM programmer and a 27C64 form the ingredients to perform an interesting trick.

The project described in Ref. 1 is a eurocard-size (10×16 cm) BASIC computer with some remarkable features, which include an on-board EPROM programmer, a machine code run option for fast turnkey applications, and a simple terminal interface. This computer is based on Intel's Type 8052AH-BASIC V1.1 single-chip microcontroller with an on-board BASIC interpreter. Interestingly, similar BASIC computers and associated development systems based on the 8052AH-BASIC were offered as ready-made units by a number of companies in the UK some time after our publication.

Many constructors of the BASIC computer have noted that the 8052AH-BASIC microcontroller is the only non-CMOS integrated circuit in the BASIC computer, and have been enquiring after a low-power equivalent to reduce the overall current consumption of the board. Unfortunately, Intel have expressed no intention to market a CMOS version of the 8052AH-BASIC.

There is, however, a way to reduce the current consumption of the BASIC computer significantly. Bearing in mind that the 8052AH-BASIC is the only member of the MCS-51® family of microprocessors and microcontrollers that has an internal ROM containing a BASIC interpreter, it should be possible to use a similar processor, a 80C32, in conjunction with an external EPROM that contains the BASIC interpreter. This replacement offers two advantages over the single 8052AH-BASIC chip: first, the current consumption of the BASIC computer is reduced from about 150 mA to 38 mA; and second, the combination of a 80C32 and an external EPROM Type 27C64 costs less than a 8052AH-BASIC. The one disadvantage should also be mentioned: the combination of the 80C32 and the 27C64 does not provide the EPROM programming facility available in the original BASIC interpreter. In most cases, however, an unmodified 8052AH-BASIC computer will remain available for writing and debugging turnkey programs. As before, these may be loaded into EPROMs for use with other systems, such as a 80C32-, 8051- or 8052-based computer.

Unloading BASIC V1.1

The general idea is simple: make a copy of the ROM-resident BASIC interpreter in the 8052AH-BASIC, and store this copy in an 8 Kbyte CMOS EPROM. Add the 80C32 and you have a low-cost CMOS equivalent of the 8052AH-BASIC.

The program listed in Fig. 1 enables the machine code that forms the BASIC interpreter in the 8052AH-BASIC to be downloaded to a terminal, or a PC that acts like a terminal. The code is formatted to the Intel-hex standard, which can be handled by almost any EPROM programmer.

The terminal connected to the BASIC computer must be VT52-, VT100-, or ANSI-compatible, and in addition provide a spool or log function. An MSDOS computer running a communications program such as Procomm® is also suitable.

Start up the BASIC computer as usual, and enter the program UPLOADER.BAS in Fig. 1 on the terminal, paying attention to the commas and other punctuation marks that are significant for the BASIC interpreter (a comma suppresses the normal CR/LF sequence). If you use a PC, type the program into your favourite wordprocessor, check it against the listing, and store it on disk in ASCII format (the PCTools wordprocessor is fine for this purpose). Next, use SENDBAS.EXE (see Ref. 1) or the communications program to transfer the file to the BASIC computer.

```
100 REM  ***********************************************
110 REM  **  INTERPRETER UPLOADER 8052-AH-BASIC V1.1   **
120 REM  **  OUTPUT FORMAT:     INTEL INTELLEC 8/MDS   **
130 REM  **                :    16 (10H) BYTES/RECORD  **
140 REM  **  VERSION       :    PJR1.0                 **
150 REM  **  DATE          :    11/10/89               **
160 REM  ***********************************************

170 STRING 2500,11
180 REM STRINGS FOR DECIMAL TO HEX CONVERSION
190 $( 0)="0": $( 1)="1": $( 2)="2": $( 3)="3"
200 $( 4)="4": $( 5)="5": $( 6)="6": $( 7)="7"
210 $( 8)="8": $( 9)="9": $(10)="A": $(11)="B"
220 $(12)="C": $(13)="D": $(14)="E": $(15)="F"
230 REM HEADER AND NUMBER OF BYTES PER RECORD
240 $(16)=":10"
250 REM NORMAL RECORDTYPE
260 $(17)="00"
270 REM LAST RECORD
280 $(18)=":00000001FF"

300 REM START UPLOADER
310 FOR BASEADDR=0000H TO 1FF0H STEP 10H
320   REM OUTPUT HEADER AND NUMBER OF BYTES PER RECORD
330   PRINT $(16),
340   REM SPLIT BASE ADDRESS IN HIGHBYTE AND LOWBYTE
350   HIGHBYTE=(BASEADDR.AND.0FF00H)/256
360   LOWBYTE =(BASEADDR.AND. 00FFH)
370   REM OUTPUT BASE ADDRESS
380   OUT=HIGHBYTE: GOSUB 1000
390   OUT=LOWBYTE : GOSUB 1000
400   REM OUTPUT RECORDTYPE
410   PRINT $(17),
420   REM INITIATE CHECKSUM
430   SUM=10H+HIGHBYTE+LOWBYTE
440   REM READ 16 INTERPRETER BYTES STARTING FROM BASE ADDRESS
450   FOR OFFSET=00H TO 0FH
460     REM READ AND OUTPUT BYTE
470     OUT=CBY(BASEADDR+OFFSET): GOSUB 1000
480     REM UPDATE CHECKSUM
490     SUM=SUM+OUT
500   NEXT OFFSET
510   REM CALCULATE AND OUTPUT CHECKSUM
520   SUM=(NOT(SUM)+1).AND.00FFH
530   OUT=SUM: GOSUB 1000
540   REM PREPARE NEXT RECORD
550   PRINT
560 NEXT BASEADDR
570 REM OUTPUT LAST RECORD
580 PRINT $(18)
590 END

1000 REM HEX OUTPUT ROUTINE
1010 REM ******************
1020 REM CONVERT 'OUT' INTO A HEX-PAIR (HIGHN,LOWN) AND OUTPUT THE CHARACTERS
1030 HIGHN=INT(OUT/16)
1040 LOWN =OUT-HIGHN*16
1050 PRINT $(HIGHN),$(LOWN),
1060 RETURN
```

900009 - 11

Fig. 1. Listing of UPLOADER.BAS, a program that enables the ROM-resident BASIC interpreter in the 8052AH-BASIC microcontroller to be copied to a PC or terminal.

```
:1000000061873720312DC0D0024003C0D0202E1090
:10001000002400B20122BC0D0024013C0D0021F7828
:1000200000218FCC0D0201F1C024023C0D002402B6D
:1000300002193620260BC29630B2FDD2963202202E
:10004000040D21632022050177E120E0FE00FD60457
:100050009506D206B9069F13971316119B173813EE
:10006000F517131483146F1478138C13C613D2135B
.......
       .......
              .......
                     .......
                            .......
                                   .......
                                          .......
:101FC00045204E554D4245522250524F4D204D4FC7
:101FD0004445222A4D43532D353128746D29204222
:101FE00041534943205631 2E312A22B16CB43A0074
:101FF000400122B43000B3224552524F523A2022BF
:00000001FF
```

900009 - 13

Fig. 2. Hexdump of the start and end of the Intel-hex file sent by the BASIC computer.

Experienced users of the BASIC computer may also consider having the 8052AH-BASIC store the program in EPROM.

Turn on the log function of the terminal, or the download function of the comms program on the PC, and type command RUN. An Intel-hex file is subsequently sent from the BASIC computer to the terminal or PC. When reception is complete, save the file, then examine it with a wordprocessor. Go to the beginning and remove the command RUN, which has been loaded because the log (download) function was active at the time it was typed. Save the corrected file.

The downloaded file is 23,054 bytes long, and ready for uploading to an EPROM programmer that can handle the Intel-hex file format. The hexdump in Fig 2 shows the start and the end of the file for reference purposes (the RUN command has been removed). Check the listed bytes against those in your file to make sure this has been loaded correctly.

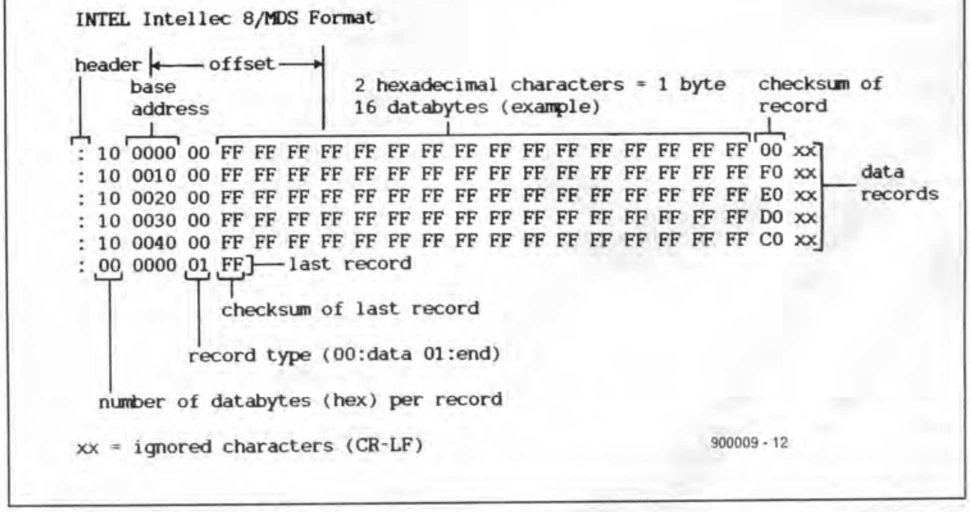
About the Intel-hex format

Although the Intel-hex format is supported by most commercially available EPROM programmers, some users of the BASIC computer may require details on the file structure to write a conversion program that converts the file downloaded from the BASIC computer into binary format.

As shown in Fig. 3, an Intel-hex file consists of records that in turn consist of 16 (10H) databytes. All numbers are in hexadecimal. Each record starts with a header, which consists of a colon (:) and a byte that indicates the number of databytes in the record. This byte can have a value smaller than 10H (16D) only in the last record. The header is followed by the address of the record. For all records except the last one, this address is incremented in 16-byte steps, although it is possible to skip certain portions of the address range. The function of the 'record type' byte is clear from the drawing. The checksum record that follows the 16 databytes is the least significant byte of the two's complement of all the bytes in the record from the byte count number to the last databyte. The last record is marked by the '01' type marker. In the example shown in Fig. 2, it contains no databytes.

Hardware

Assuming that a Type 2764 EPROM has been successfully loaded with the interpreter code, it is time to turn to the hardware of the BASIC computer.


INTEL Intellec 8/MDS Format
header
offset
base address
2 hexadecimal characters = 1 byte
16 databytes (example)
checksum of record
data records
last record
checksum of last record
record type (00:data 01:end)
number of databytes (hex) per record
xx = ignored characters (CR-LF)
900009 - 12

```
: 10 0000 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF 00 xx
: 10 0010 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF F0 xx
: 10 0020 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF E0 xx
: 10 0030 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF D0 xx
: 10 0040 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF C0 xx
: 00 0000 01 FF
```

Fig. 3. Intel-hex record format.

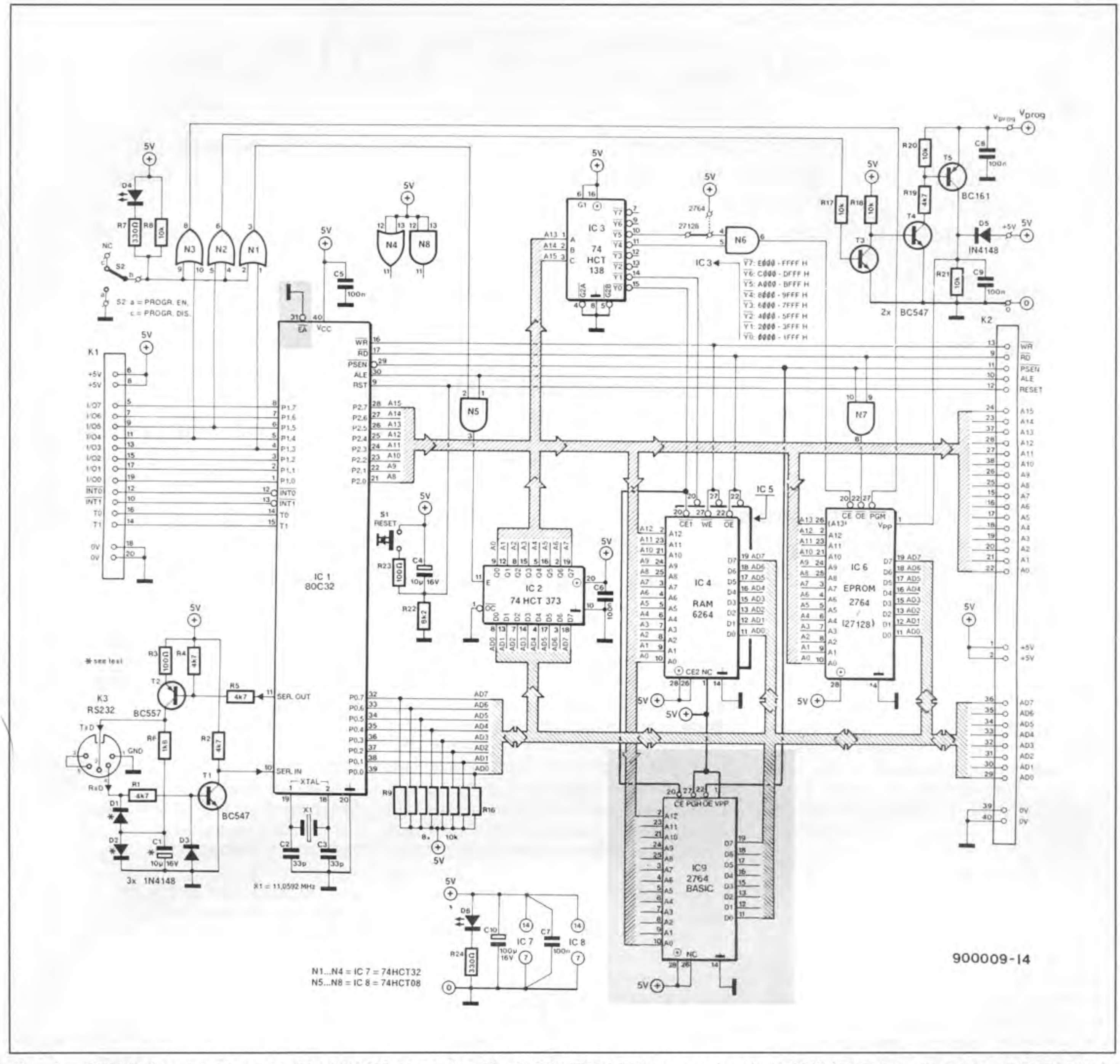


Fig. 4. Circuit diagram of the modified BASIC computer. The 27C64 EPROM that contains the BASIC interpreter is connected virtually in parallel with the existing system RAM, IC4.

The circuit diagram in Fig. 4 shows the changes made to the BASIC computer. The 8052AH-BASIC has been replaced with an 80C32 of which pin 31 is connected to ground. Cut the track from pin 31 to the supply voltage, and connect pin 31 to ground with the aid of a small piece of wire. With the exception of two pins, the EPROM that contains the BASIC interpreter has the same connections as the 8 Kbyte RAM used in location IC$_4$. A 28-way IC socket is mounted piggy-back on to IC$_4$, but pins 22 and 27 of the socket are bent aside (i.e., they are not connected to the corresponding RAM pins). Socket pin 27 is connected to socket pin 28, and the two are connected to RAM pin 28. Socket pin 22 is connected to pin 29, $\overline{\text{PSEN}}$ of the microcontroller. Finally, connect pin 1 of IC$_4$ to the positive supply with the aid of a short piece of wire. The +5 V track runs nearby pin 1 at the track side of the board.

Ready for use

Remove the 8052AH-BASIC from its socket and replace it by the 80C32. Mount the programmed 27C64 in the socket on top of IC$_4$. Connect the computer to the terminal or PC, apply power, and press the space bar to get the system on line. If everything is all right, the computer sends the message

```
*MCS-51(tm) BASIC V1.1
READY
>
```

You are now ready to use the BASIC computer. Remember, however, that the EPROM programming facility is no longer available in BASIC. Switch S$_2$ on the board must, therefore, left in the 'program disable' position.

Reference:

1. BASIC computer. *Elektor Electronics* November 1987.

For further reading:

1. Single-chip microcontrollers. *Elektor Electronics* September 1987.
2. Peripheral modules for BASIC computer. *Elektor Electronics* October 1988.

INTERMEDIATE PROJECT

A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.

7. One-wire intercom

J. Bareford

This month's project is a long-distance intercom system that can be set up very quickly for outdoor events because a large number of extensions can communicate via a single, light-duty wire.

The intercom is intended for outdoor events and games such as rallies, camping parties, scrambles, etc., where a simple means of communication is required between extensions 'in the field'. Contrary to most other intercom systems, the circuit presented here is uncritical of the wire type used. Furthermore, the current consumption of each extension is remarkably low when none of the other posts is speaking, so that batteries may be used to supply the power. The system is open, that is, all extensions receive all communication on the line.

The remarkable thing about the intercom is, of course, that it requires a single wire only. The secret is that the return connection (normally a separate ground wire), is formed by the soil between the extensions, or, more precisely, the resistance formed by the soil. Depending on the soil structure, a resistance of between 10 kΩ and 100 kΩ may be measured between two metal pins pushed approximately 30 cm into the ground at a distance of few metres. Interestingly, this resistance does not rise in direct proportion to the pin distance.

The circuit

For obvious reasons, the design of the intercom is based on the presence of a relatively high resistance of the ground return path between the extensions. This means that the transmitter part of the circuit must provide sufficient voltage gain, while the receiver must have a relatively high input impedance. A circuit that meets these requirements while remaining as simple as possible is shown in Fig. 1. Only three transistors, a small loudspeaker, a three-pole rotary switch and a handful of passive components are required for each extension.

With the switch positioned as shown, the intercom is set to 'listen'. Signals from other extensions are taken from the field communication line, j-k, and arrive at the base of T_1 via pole 'a' of S_1. In the 'listen' mode, the three transistors form a kind of super emitter follower with a very high input impedance (several MΩ) to compensate the resistance formed by the earth

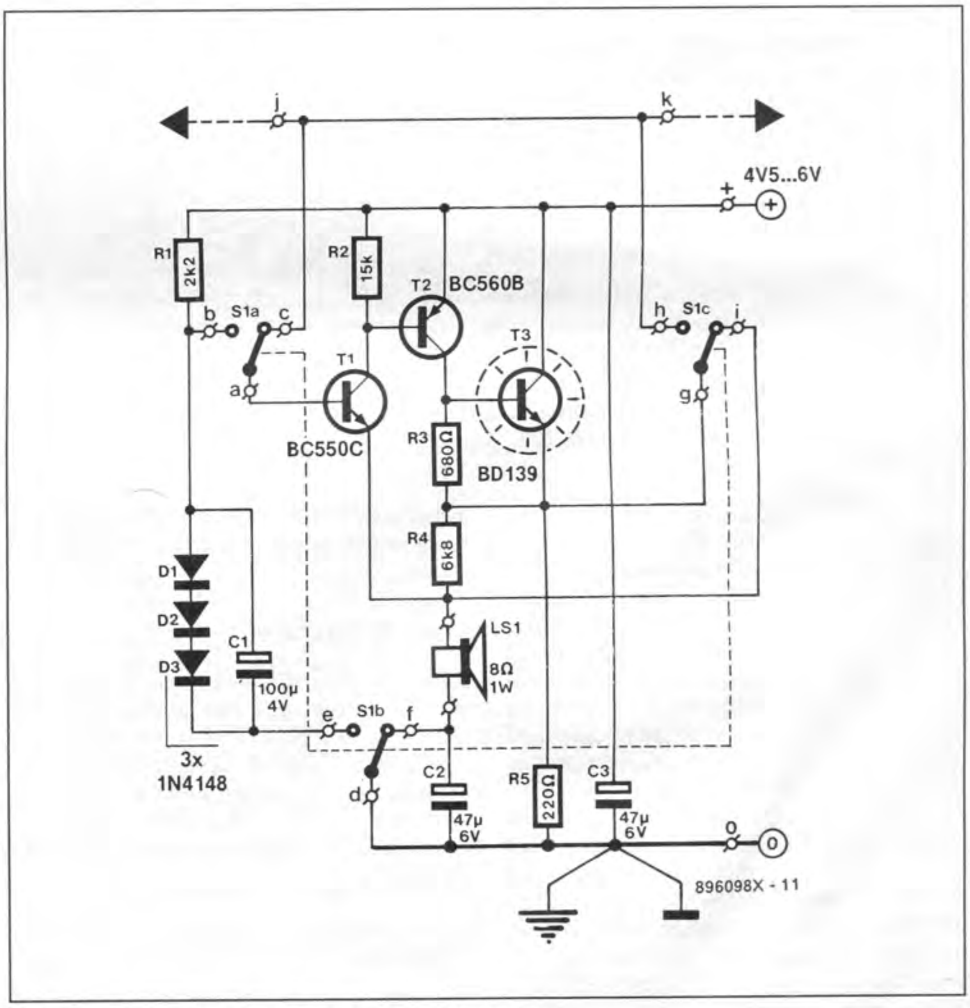


Fig. 1. **Circuit diagram of an intercom extension.**

return path. Switch contact S_{1c} connects the loudspeaker between the emitter of T_3 and ground.

Some readers may object at this stage by saying that the amplifier composed of T_1-T_2-T_3 can never work because there is no base voltage on T_1. This is correct, but only as long as there is no signal on the line. Hence, the unit draws a very low stand-by current.

T_1 does not receive base voltage from the line until one of the other extensions starts transmitting when S_1 is operated. Let's look at what happens at the transmitting extension. Effectively, the three transistors still function as an amplifier, but with the loudspeaker acting as a microphone. In the 'receive' mode, T_1 functions as an emitter follower. In the 'transmit' mode, however, its base is held at a fixed potential provided by R_1-D_1-D_2-D_3. Since AF signals are decoupled by C_1 at the base of T_1, the transistor operates in a grounded-base configuration that provides considerable amplification of the microphone signal applied to the emitter. T_2 and T_3 raise the signal to a level suitable for applying to line j-k.

Negative feedback required to ensure stable gain with acceptable distortion is provided by resistor R_4, which is connected between the amplifier output (emitter of T_3) and the amplifier input (emitter of T_1). The total voltage gain is, therefore, determined by the ratio R_4/Z_{Ls-1}, which works out at about 850.

The amplifier output is coupled direct to line j-k, and the resultant direct voltage serves as the previously mentioned base voltage for T_1 in every extension switched to the 'listen' mode. The direct voltage is about equal to the forward drop across D_1-D_2-D_3 (about 1.8 V), minus the base voltage of T_1, and plus the voltage on R_4. In all, this works out at about 1.5 V, independent of the supply voltage. This voltage is sufficient to make T_1 in the extension(s) conduct, while preventing unduly high loudspeaker currents.

Let's build it

A suggested construction of the intercom circuit on Universal Prototyping Board Size-1 (UPBS-1) is shown in Fig. 2. Stick closely to the Parts List and the component mounting plan, and you will find that construction is straightforward. Do not forget the wire links, and be sure to observe the polarity of the electrolytic capacitors and the orientation of the transistors. Fit power transistor T_3 with a small heat-sink.

The loudspeaker and the rotary switch are external components, which are connected to the board via short wires and solder pins with letter codes in the case of the switch. Cut the field communication line at the location of the extension, and connect the wire ends to points 'j' and 'k' on the PCB.

As already stated, the intercom extension has a modest current consumption, so that it may be powered from three or four series-connected penlight batteries, or a single 4.5 V type. The completed board and the battery or batteries are fitted into a suitably sized ABS enclosure with a listen/talk switch and two wander sockets for the speech line and the earth connection.

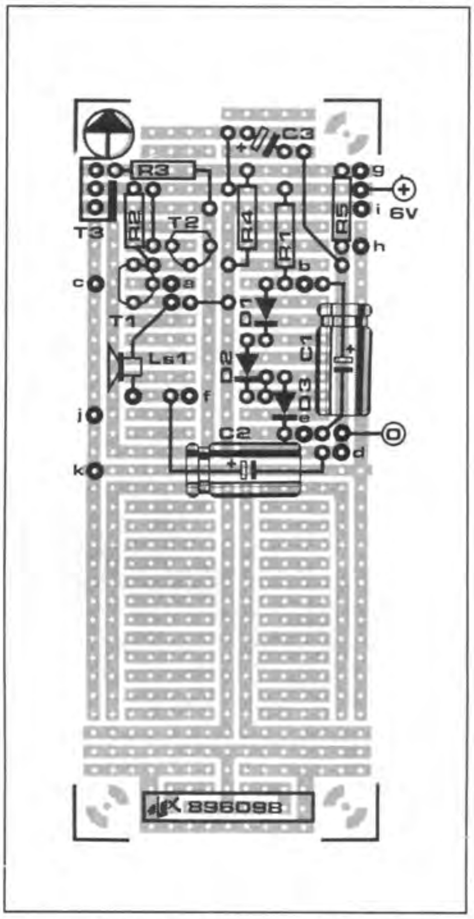


Fig. 2. Suggested construction of an intercom extension on ready-made prototyping board UPBS-1.

Parts list

Resistors:
R_1 = 2k2
R_2 = 15k
R_3 = 680Ω
R_4 = 6k8
R_5 = 220Ω

Capacitors:
C_1 = 100µ; 4 V
C_2;C_3 = 47µ; 6 V

Semiconductors:
D_1;D_2;D_3 = 1N4148
T_1 = BC550C
T_2 = BC560C
T_3 = BD139

Miscellaneous:
S_1 = three-pole changeover switch.
Loudspeaker 8Ω; 1 W.
Heat-sink for T_3.
PCB Type UPBS-1 (see Readers Services page).

HCMOS OSCILLATORS

by J. Ruffell

HCMOS integrated circuits were originally intended for the design of fast, low-power-consumption digital circuits. In practice, these devices have proved to be suitable for a number of other applications as well. This article describes how they may be used in the design of simple, yet reliable, *RC* and crystal oscillators.

HCMOS integrated circuits are devices that work fast, are economical in power consumption, operate without any problems from a range of supply voltages, and have a threshold voltage that is pretty stable over a wide range of operating temperatures. These parameters make them eminently suitable for designing stable, reliable oscillators. In practice, these oscillators are normally of the *RC* type; if very stable and precisely defined frequencies are needed, the *RC* network must be replaced by a crystal.

Because HCMOS gates possess a very high input impedance, capacitors with a wide range of values may be used in the *RC* network. Even more important is perhaps that capacitors of very low value may be used, so that little energy is lost during operation.

Basic circuit

The basic circuit of an oscillator designed from two inverters and the waveforms that occur in the circuit are shown in Fig. 1. Because of the inversion in the two gates, it is certain that the polarity of the voltages at A and B is opposite to that of the potential at C.

To keep the description simple, it will be assumed that the potential at A and B is low and that at C is high. Capacitor *C* is charged via resistor *R* until the voltage at B reaches the switching level of the inverter, V_{ST}. The potential at C then becomes low and that at A high.

Since the level at the output varies rapidly, the level of the potential at B should become $V_{ST} + V_{CC}$. However, the input of the inverter is protected by a diode, so that the voltage at B can not exceed $V_{CC} + V_D$, in which V_D is the potential drop across the diode. Conversely, the maximum level of the negative voltage in the circuit can not exceed $0 - V_D$, and this occurs when the output of inverter 2 becomes low. The voltage at B rises from that level to V_{ST}; only when that level is reached, does the output of inverter 1 become low again. The time constant, $\tau = RC$, determines the charging and discharging periods of the capacitor:

$$\tau_1 = -RC \ln\{V_{ST}/(V_{CC} + V_D)\}; \qquad [1]$$

$$\tau_2 = -RC \ln\{(V_{CC} - V_{ST})/(V_{CC} + V_D)\}; \qquad [2]$$

$$f = 1/(\tau_1 + \tau_2). \qquad [3]$$

The values of τ are in seconds and that of *f*, the frequency at which the oscillator begins to operate, is in hertz.

External influences

For Type 74HC/HCU circuits, the manufacturers state that V_{ST} is typically half the supply voltage, V_{CC}. Since $V_D = 0.7$ V, a quick calculation shows that the frequency drift varies from +9% to −2.5% if the 5 V supply voltage varies from 3 V to 6 V. The inequality of the positive and negative drift is caused by the constancy of the potential drop across the diode, irrespective of the level of the supply voltage. This constancy is important in the calculation of τ_1, because the term in brackets in formula [1] will vary when the supply voltage varies in spite of V_{ST} being a fixed percentage of the supply voltage. The frequency vs supply voltage characteristic is given in Fig. 2.

Although the manufacturers state that the threshold voltage is typically 0.5 V_{CC}, in practice it appears that its value lies between 0.3 and 0.7 in case of the HC family and between 0.2 and 0.8 in case of the HCU family. This means that the frequency drift of HC oscillators is not greater than 9.5%, but that of HCU oscillators may be as high as 21.5%.

The frequency vs threshold voltage

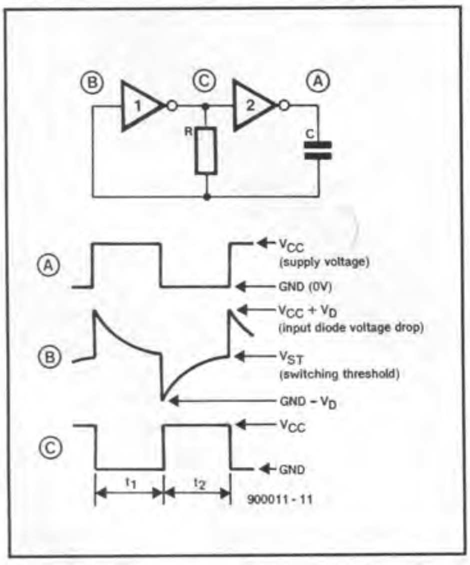


Fig. 1. Basic circuit of an *RC* oscillator designed from two digital inverters.

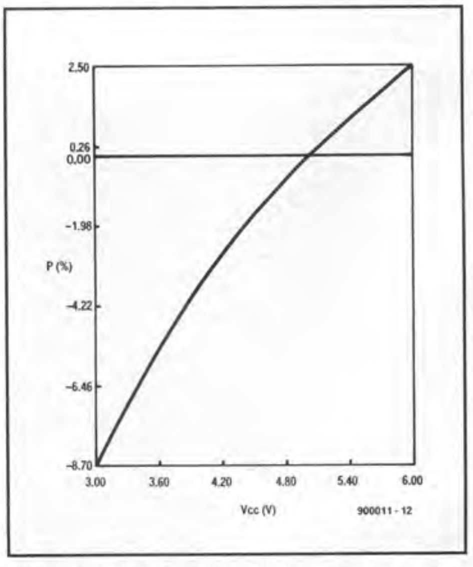


Fig. 2. Oscillator frequency vs supply voltage.

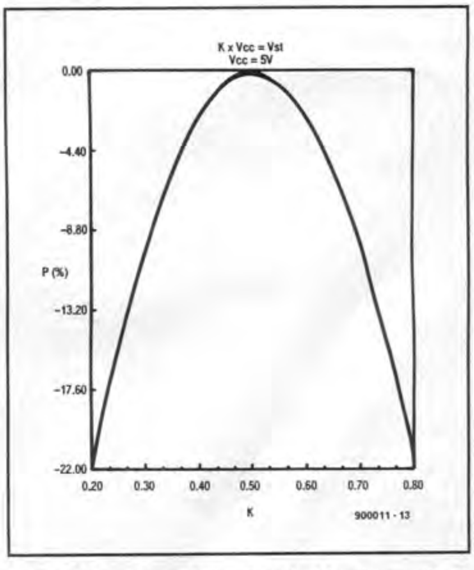


Fig. 3. Variations of the threshold voltage affect the oscillator frequency.

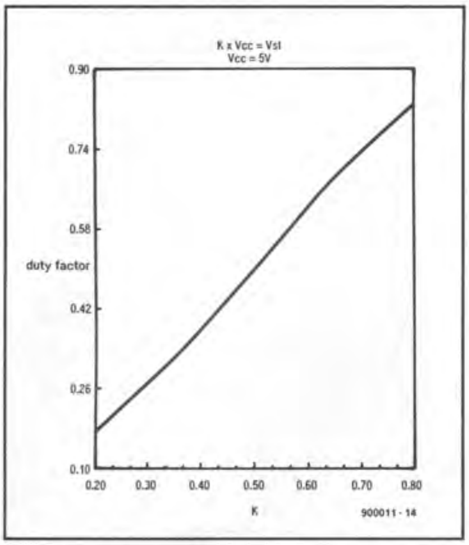


Fig. 4. In *RC* oscillators designed around HC or HCU inverters, the duty factor is highly dependent on the level of the threshold voltage.

characteristic is given in Fig. 3. It is interesting to note that a deviation of the threshold voltage from its nominal value always results in a lowering of the frequency. As shown in Fig. 4, the duty factor is also affected by such a deviation; only in the ideal case, that is, when the threshold voltage is equal to half the supply voltage, will the duty factor be 50%.

In the above, ICs from the HCT family have not been considered, because their switching behaviour is rather more precise than that of devices in the other two families. Moreover, HCT circuits may be used only with supply voltages of 4.5–5.5 V, and with these the threshold voltage varies relatively little.This results in a maximum frequency drift of not more than ±0.8% over the specified operating range, while the duty factor remains fairly constant at around 75%. The asymmetric behaviour here is caused by the threshold voltage not being centred around half the supply voltage. In practice, it is found that the maximum deviation of the threshold voltage, when the supply voltage is 5 V, causes a frequency drift of not greater than 16%.

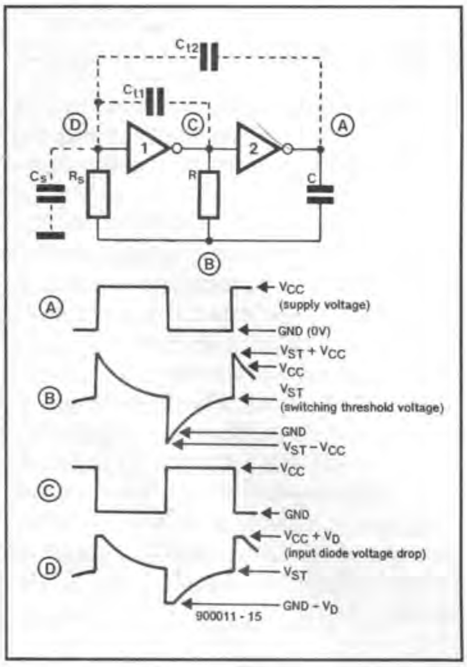


Fig. 5. A second resistor makes the oscillator far more stable.

Improved stability

Adding a resistor, *R*s, to increase the input impedance of inverter 1, as shown in Fig. 5, makes the circuit a great deal more stable. The additional resistance increases the discharge period of capacitor *C*, and causes the threshold voltage of the protection diode to have less influence on the operation of the circuit. If the value of *R*s is chosen high enough, the waveforms shown in Fig. 5 will ensue. Note that the voltage at B varies around the threshold voltage at a value equal to *V*CC. Too low a value of *R*s may result in clipping of the voltage peaks, while too high a value may, in conjunction with *C*t1, cause spurious oscillations. At an optimum value of the resistor, the variations of the duty factor and the frequency are reduced by some 30%, irrespective of whether HC, HCT or HCU devices are used.

It appears that ICs in the 74HCU series, because their outputs are not buffered, are particularly suitable for this type of oscillator.

In general, it appears that the optimum value of *R*s is equal to 2*R*. At this value of *R*s, the time constants are:

$$\tau_1 = -RC \ln\{V_{ST}/(V_{CC} + V_{ST})\}; \qquad [4]$$

$$\tau_2 = -RC \ln\{(V_{CC} - V_{ST})/(2V_{CC} - V_{ST})\} \quad [5]$$

while the period of oscillation, *T*, is:

$$T = -RC \ln\left[\frac{V_{ST}(V_{CC} - V_{ST})}{(V_{CC} + V_{ST})(2V_{CC} - V_{ST})}\right] \qquad [6]$$

From this formula, it is seen that the diode voltage no longer affects the period. If ICs from the 74HC or 74HCU families are used, so that *V*ST is roughly 0.5*V*CC,

$$T = 2.2RC. \qquad [7]$$

Because of the different value of *V*ST in HCT circuits (where it has a fixed value and is not a percentage of the supply voltage), a small correction is necessary and this makes the period:

$$T = 2.4RC. \qquad [8]$$

Formulas [7] and [8] are approximations, but in practice they prove to be very close to the measured value. The measured and calculated values are summarized in Table 1 (in which *R*s = 2*R*).

The astable multivibrator functions well if bipolar capacitors with a value of not less than 100 pF are used. Moreover, formulas [7] and [8] are usable only if the parasitic capacitances may be ignored: this is so when the capacitor is greater than 10 nF. Resistor *R* may have a value of between 1 kΩ and 1MΩ.

Use of crystal

If a very stable oscillator is needed, it should be controlled by a crystal instead of an *RC* network. A crystal has the further advantage that it is much more suitable than *RC* networks for generating high frequencies. Also, if a crystal is used in an HCMOS circuit, it requires very little power. This explains the popularity of

	τ	*T* (computed)	*T*=2.2τ	*T* (measured)
74 HC	1000	2174	2200	2177
*V*CC = 5 V	100	217	220	218
*V*ST = 2.5 V	10	21.7	22	22.6
	1	2.17	2.2	2.4
	0.1	0.217	0.22	0.3
74HCU	1000	2174	2200	2147
*V*CC = 5 V	100	217	220	214
*V*ST = 2.5 V	10	21.7	22	21.7
	1	2.17	2.2	2.4
	0.1	0.217	0.22	0.3
			T=2.4τ	
74HCT	1000	2348	2400	2362
*V*CC = 5 V	100	235	240	236
*V*ST = 1.415 V	10	23.5	24	24.4
	1	2.35	2.4	2.6
	0.1	0.235	0.24	0.3

Table. 1. In practice, the difference between computed and measured values is found to be small.

HCMOS / crystal oscillators.

The electrical equivalent of a crystal is shown in Fig. 6. It consists of an inductance, a resistance and two capacitances.

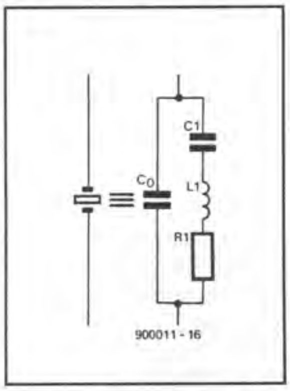


Fig. 6. Equivalent electrical circuit of a crystal.

The circuit has a series- as well as a parallel-resonant frequency, and this must be borne in mind during the design of the oscillator. The crystal manufacturer always indicates whether a crystal has been cut for series or parallel operation. In the final instance, the position and value of capacitance C_L determine in which mode the crystal will oscillate (see Fig. 7).

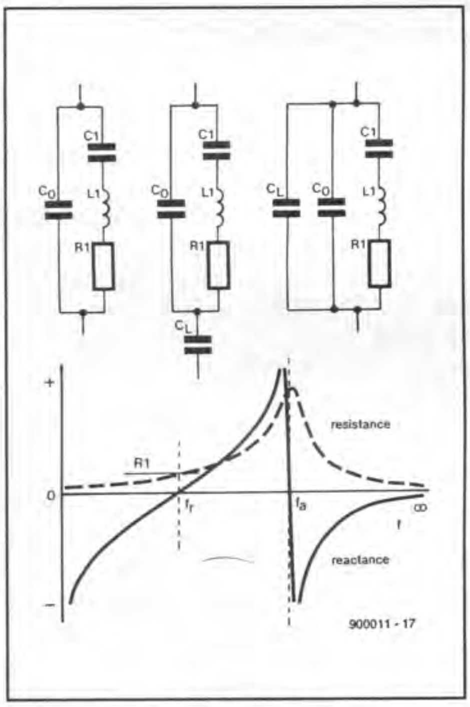


Fig. 7. Dependent on the load, a crystal may jump from one mode of operation to another. At the left, the equivalent circuit of the crystal; at the centre, the equivalent circuit for series-resonant operation; at the right, the equivalent circuit for parallel-resonant operation.

Series-resonant oscillators are designed to oscillate near the resonance frequency, f_r, of the crystal. Parallel-resonant oscillators operate at a frequency that depends on the capacitance of the shunt capacitor and lies somewhere between f_r and the so-called anti-resonance frequency, f_a. This is the reason that in practical circuits part of the load capacitance is formed by a variable capacitor.

The Pierce oscillator in Fig. 8 uses a Type 74HCU04 chip (which is not buffered since buffered devices can not be used here). Boffins will recognize the circuit as a Colpitts oscillator in which the inductance has been replaced by a crystal. This type of oscillator uses very little power and offers good suppression of third harmonics.

The latter characteristic is important, because many oscillators have a tendency to jump to harmonic frequencies.

Although the circuit may be used with a supply voltage of 2 V, it is recommended not to use supplies below about 3 V. The maximum supply voltage is 6 V.

Owing to the low output impedance of the ICs, they can not be connected direct to the crystal, and it is, therefore, necessary, to add a resistance in the output to raise the impedance. Unfortunately, this resistance may introduce a phase shift, and its use above 4 MHz is, therefore, not recommended. Instead, a capacitance must be used: the value of this for use with most crystals is about 30 pF. Here, since C_{L1} and C_{L2} are in series, the buffer capacitor should have a value of about 56 pF.

For optimum operation of the Pierce oscillator, its output impedance must be equal to the impedance of the frequency-determing network. This load impedance, Z_L is approximately

$$Z_L = X_{CL}^2/R_r \qquad [9]$$

in which X_{CL} is the reactance of capacitor C_{L2} and R_r is the resistance of the crystal at resonance: in practice, this is 75 Ω.

In theory, the optimum value of R_L in a 4 MHz oscillator is 5900 Ω, whereas the impedance of the output gate is only about 40 Ω. A practical value of 5600 Ω results in too high a phase shift: a compromise value is found to be 2200 Ω.

Resistor R_f sets the DC operating point of the amplifier; its value is not critical: between 1 MΩ and 10 MΩ is fine.

Gate delay

Every gate in an IC has a certain delay, t_p, which in fast HCUMOS gates amounts to about 14 ns. This delay causes a small phase shift, Φ, between the input and output signal, which at high frequencies can not be ignored. The shift is calculated from:

$$\Phi = f\,t_p \times 360° \qquad [10]$$

At an oscillator frequency of 6 MHz, the delay causes a phase shift of about 30° which, coupled with the phase shift introduced by R_S, causes the Pierce oscillator to stop. If the resistor is replaced by a capacitor whose value is equal to that of C_L, the total phase shift is brought back to a value that allows the oscillator to work correctly.

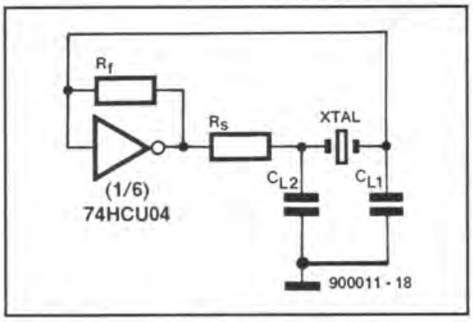


Fig. 8. Basic circuit of a Pierce oscillator using only one gate. Two additional resistors ensure that the gate operates as an amplifier. Resistor R_f provides the DC operating point of the amplifier.

Finally

Crystal manufacturers cut crystals for use in high-frequency oscillators in a manner that allows the crystals to oscillate at an harmonic. Crystals for operation at 10–75 MHz oscillate at the third overtone. At higher frequencies, 50–125 MHz, crystals are used that oscillate at the fifth harmonic.

To use these crystals, the circuit needs a small modification as shown in Fig. 9.

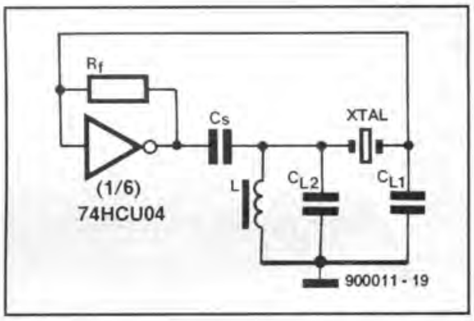


Fig. 9. This small modification ensures that the circuit operates satisfactorily with crystals that are intended for operation at harmonic frequencies.

The modification ensures suppression of the fundamental frequency in two ways. Capacitor C_S has a value that is about equal to that of C_L and thus presents a higher impedance to the fundamental than to the third overtone. The circuit consisting of L and C_S oscillates at a frequency that is slightly lower than the third overtone. Adjusting L for maximum output voltage may cause a small change in the oscillator frequency, but this may be trimmed out by C_L, which in practice will consist of a fixed and a variable capacitor.

ONE-PAGE A4 MONITOR FOR DTP AND CAD

Samsung have recently introduced a low-cost, 15-inch monochrome display that is ideally suited to entry-level DTP (desktop publishing) applications, CAD (computer-assisted design) and wordprocessing.

The monitor allows full-size A4 pages to be previewed at a resolution of 768:1008 pixels. The vertical and horizontal scan frequencies are 60 Hz and 63 kHz respectively to ensure a dense and flicker-free image.

The monitor comes with a display adapter card for IBM PCs and compatibles. This card may be configured to emulate the Hercules graphics card, but can also operate alongside it.

Software drivers are provided for recent releases of major PC programs, including Autocad, GEM/3, Symphony, Lotus 1-2-3, Ventura Publisher, MS Windows/286/386, Pagemaker, Wordstar and WordPerfect.

A review sample of the monitor supplied to us by Samsung UK was tested with WordPerfect 5.0 and Ventura 2.0 Professional. This gave excellent results and compared favourably to a number of far more expensive A4 monitors. We particularly appreciated the non-glare screen, the short screen redrawing time and the ease of installing the card and the associated software on the test compter, a NEAT-286, 20 MHz, AT compatible.

The monitor was supplied by **Samsung Electronics (UK) Ltd, Unit 1, Hook Rise Business Industrial Centre, 225 Hook Rise South, SURBITON KT6 7LD. Telephone 01-391 0168; Fax 01-397 9949.**